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A 2.5 mW D-Band Broadband Simultaneous Noise- and Input-Matched InP LNA

Sehoon Park[1] | Yang Zhang[2] | Arno Hemelhof[2,3] | Kristof Vaesen[2] | Mark Ingels[2] | Piet Wambacq[2,3]

[1]School of Electronic and Electrical Engineering, Kyungpook National University, Daegu, South Korea | [2]IMEC, Leuven, Belgium | [3]Department of Electronics and Informatics, Vrije Universiteit Brussel, Brussels, Belgium

Correspondence: Yang Zhang (yang.zhang@imec.be)

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ABSTRACT

A D-band ultra-low-power and broadband two-stage, gain-boosted low-noise amplifier (LNA) in a 250-nm InP DHBT process is presented. The LNA adopts a simultaneous noise and input matching technique, minimizing loss at the input while boosting the gain over a broad frequency range. The gain boosting core uses a feedback network based on a long transmission line between the base and collector and feedback at the emitter to satisfy the gain, stability and bandwidth requirements at once. The LNA achieves 6.2 dB noise figure, 27 dB gain between 130 and 155 GHz while consuming only 2.5 mW DC power.

1 | Introduction

The rapid growth in data demand along with emerging applications, such as AI, AR/VR and 3D holograms pushes the operating frequency of wireless communication systems to the D-band (110–170 GHz), which offers broad bandwidths. The high path loss and the degraded transistor performance at high frequencies, however, challenge the design of D-band front-ends. CMOS technologies with a limited f_{max} and supply voltage, require a large number of amplifiers with high power consumption to obtain sufficient gain and output power [1].

As an alternative to CMOS, InP devices exhibit much higher gain, efficiency and breakdown voltage with higher f_t/f_{max}. This unique advantage makes the InP technology a key enabler of future communication systems. While InP power amplifiers clearly outperform their CMOS counterparts for operation above 100 GHz, the advantage of InP for LNAs has not yet been fully exploited [2].

Given the limited output power of a D-band transmitter, the link distance can be improved by having a low-noise, high-gain and low-power LNA, which then determines the sensitivity of the full RX chain. Since the optimal impedances for the noise and gain of a single transistor generally occur at different positions, a trade-off is needed here. In the CMOS LNA of [3] source degeneration is used to bring the optimal impedance for gain and noise figure (NF) closer to each other. This idea reduces the loss and NF degradation from the input matching network while still reducing the gain of the transistor core itself. In [4] a gain boosting technique is applied to exploit the maximum achievable gain (G_{max}) of a transistor by manipulating the feedback and the input impedance to obtain simultaneous noise and input matching (SNIM). This method avoids a gain drop and achieves a low NF but it comes with a narrow bandwidth. Further, the LNA in [5] improves the bandwidth at the expense of gain which in turn exhibits a similar figure-of-merit (FoM) with the LNA in [4].

This work proposes a two-stage broadband SNIM LNA with ultra-low DC power consumption. To fully exploit the high gain potential of the available InP DHBT technology, a broadband gain-boosting technique is applied. The design employs two high-order feedback paths at the base–collector and emitter to simultaneously satisfy the gain, stability and bandwidth requirements while avoiding hard trade-offs. In particular, a long and lossy transmission line ($> \lambda/4$) in the base–collector feedback path,

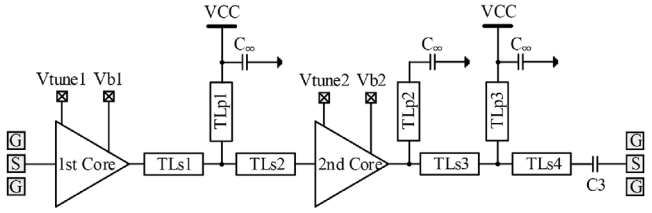

FIGURE 1 | Proposed two-stage LNA. The input matching is contained inside the first amplifier core. Interstage and output matching networks contain series transmission lines TL [1..4] and parallel lines TLp[1..3]. Capacitors C_∞ are decoupling capacitors.

together with a series capacitor, generates a negative resistance that compensates passive losses and enhances the overall gain. The amount of positive feedback in the base–collector path is further controlled by tunable transmission lines (TL) to partially recover unexpected variations.

2 | Circuit Implementation

Figures 1 and 2 show the schematic of the proposed two-stage LNA and its transistor core, respectively. The circuit is implemented in a single-ended fashion with a TL-based matching network. The TLs in this design are made with microstrip lines and they are separated far enough from each other to avoid mutual coupling. Both the first and the second stage exploit positive feedback to boost the gain and to adjust the impedance for minimum interstage matching loss and NF degradation. A varactor (V1) is coupled to the positive feedback path for the transistor core to fine tune the amount of feedback.

2.1 | Design of Gain-Boosting Core

The transistor cores employ a gain-boosting technique to achieve sufficient power gain close to G_{max}. Conventional gain-boosting cores face significant trade-offs between gain, bandwidth, stability and the simultaneous noise and input matching for the LNA design. Furthermore, resistive losses in the feedback network reduce the unilateral gain, diminishing the advantages of the gain boosting. To overcome these design challenges, the amplifier core presented in this paper uses two feedback paths around the amplifying transistor: one from the collector to the base and one between emitter and ground. The feedback networks are implemented with high-order passive networks composed of TLs longer than a quarter wavelength, combined with series and shunt capacitors (see Figure 2). Further, the transmission line in the feedback network between collector and base is made tunable, allowing to control the amount of the positive feedback.

The first (positive) feedback path, between collector and base, boosts the gain. As shown in Figure 2, additional TLs (TLb1, TLc1) are inserted in series with the base and collector to achieve the desired input and output impedances [6]. Different from conventional broadband gain-boosting cores utilizing only a TL with DC blocking capacitors [7], the proposed core adds a small capacitor (Cf1) in series with the TL that has a total length longer than $\lambda/4$ (see TLf1, TLf2 and TLt1 in Figure 2).

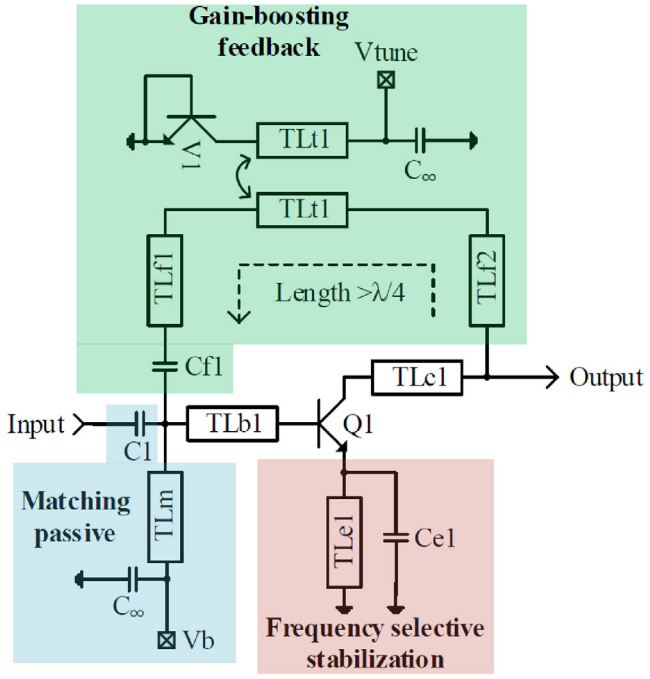

FIGURE 2 | Proposed gain-boosting core.

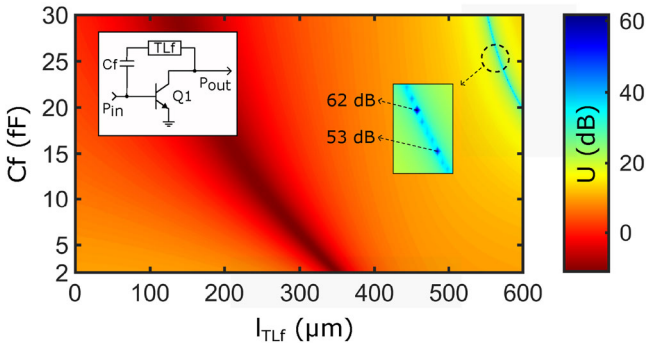

FIGURE 3 | Unilateral gain U of a gain-boosting core in the inset as a function of the capacitance Cf and the length of the lossy transmission line TLf.

Combining a capacitor with a long transmission line provides distinct advantages, as explained below.

The resistive losses from the TLs in the feedback path can be utilized to increase the unilateral gain (U) and the G_{max} of the core. This might be counterintuitive but is explained with the network shown in the inset of Figure 3, which consists of a common-emitter transistor Q1 with a series connection of a capacitor Cf and a lossy transmission line TLf between base and collector. The transistor has a size of 0.25×4 μm^2 and for the analysis here the DC voltages are $V_{BE} = 0.77\,V$ and $V_{CE} = 1\,V$. The 2-port Y-parameter representation of the cascaded Cf and TLf ($Y_{cf,TLf}$) can be expressed as:

$$Y_{cf,TLf} = \frac{1}{Z_0 \sinh(\gamma_f l_{TLf}) + Z_{cf}\cosh(\gamma_f l_{TLf}))} \times \begin{bmatrix} \cosh(\gamma_f l_{TLf}) & -1 \\ -1 & \cosh(\gamma_f l_{TLf}) + \frac{Z_{cf}}{Z_0}\sinh(\gamma_f l_{TLf}) \end{bmatrix}, \quad (1)$$

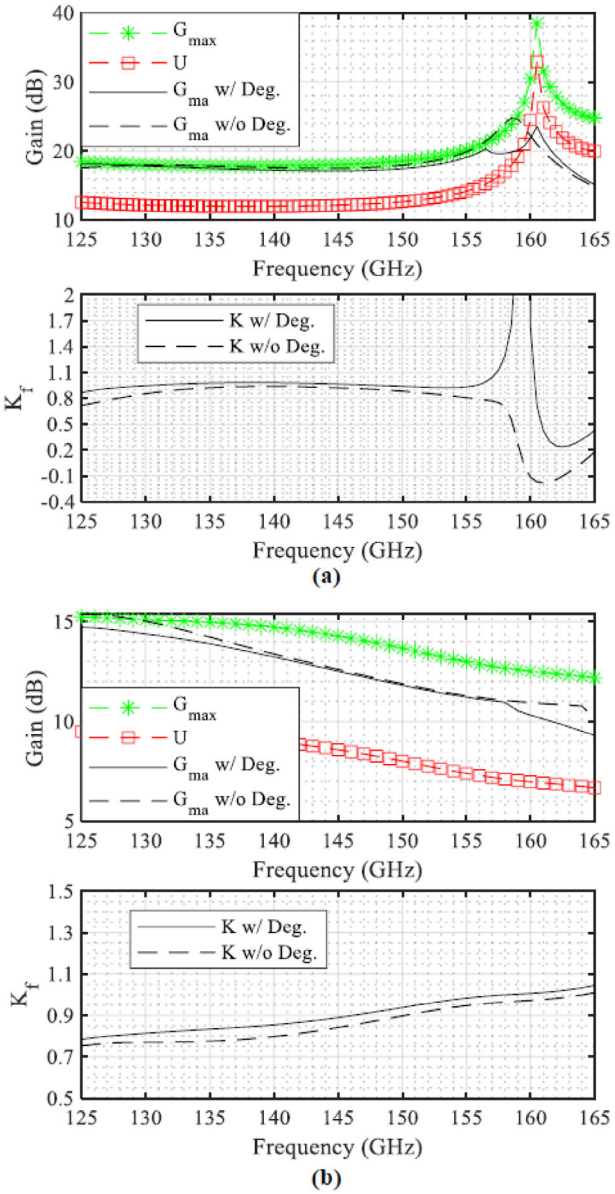

FIGURE 4 | Gain (maximum achievable gain: $G_{\max}$, unilateral gain [U], and maximum available gain [G_{ma}]) and stability factor (K_f) with and without emitter degeneration: (a) second stage and (b) first stage.

where $Z_{\mathrm{cf}} = \frac{1}{j\omega C_f}$, Z_0 is the characteristic impedance, $\gamma_f = \alpha_f + i\beta_f$ is the propagation constant for the lossy TL and l_{TLf} is the length of TLf. From (1), the real and imaginary parts of the feedback and feedforward admittance, $Y_{21,\mathrm{cf,TLf}} = Y_{12,\mathrm{cf,TLf}}$, are given by:

$$Re\{Y_{21,\mathrm{cf,TLf}}\} = -\frac{D_r}{D_r^2 + D_i^2}, \qquad \mathrm{Imag}\{Y_{21,\mathrm{cf,TLf}}\} = \frac{D_i}{D_r^2 + D_i^2},$$

$$\text{with} \quad \begin{cases} D_r = \sinh(\alpha l)\,[Z_0 \cos(\beta l) + X_{\mathrm{cf}} \sin(\beta l)], \\ D_i = \cosh(\alpha l)\,[Z_0 \sin(\beta l) - X_{\mathrm{cf}} \cos(\beta l)], \\ X_{\mathrm{cf}} = \dfrac{1}{\omega C_f}. \end{cases} \tag{2}$$

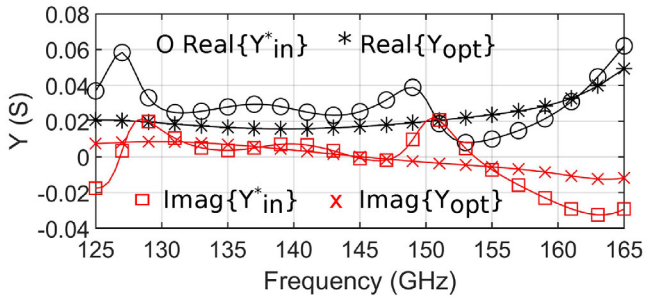

FIGURE 5 | Conjugated input admittance (Y_{in}^*) and optimal noise admittance (Y_{opt}) for the LNA.

When Cf is sufficiently small such that $X_{\mathrm{cf}} > Z_0$ in (2), the real part D_r changes sign once the electrical length $\beta_f l_{\mathrm{TLf}}$ exceeds $\pi/2$ ($> \lambda/4$), indicating that the feedback and feedforward paths introduce a negative resistance. This negative resistance substantially increases the unilateral gain U beyond that of the intrinsic transistor, effectively compensating for passive losses in the embedding network. This is confirmed by the simulated U in Figure 3 approaching a nearly infinite value (62 dB) at 140 GHz. The imaginary component D_i in (2) also reverses its sign beyond the quarter wavelength, transforming the capacitive behaviour of Cf into an inductive one. This inductive behaviour counteracts the intrinsic base–collector capacitance, stabilizing the core and providing gain boosting through the feedback path, similar to conventional inductor-based gain-boosting cores. Unlike the single inductor-based approach, the proposed high-order C_f–TL_f feedback network offers a larger design freedom, enabling broadband operation with enhanced gain performance and reduced passive losses due to the negative resistance at feedback, which are otherwise unavoidable in conventional $G_{\max}$ cores.

The insights from the analysis of the network of Figure 3 are used in the gain-boosting core of Figure 2. Here, the negative resistance in the feedback between collector and base of the amplifying transistor in each stage is used to compensate the losses in TLb1, TLc1, TLe1, Ce1 and TLm. Furthermore, this negative resistance allows the incorporation of a coupled varactor (V1, TLt1) in the feedback path, in contrast to conventional gain-boosting cores that exclude such varactors due to their large loss. This varactor, implemented as a reversely biased base–collector diode, provides a wider tuning range and a higher quality factor than a base–emitter diode topology, as demonstrated in [8]. It offers tunability by controlling the capacitance coupled to TLt1 and by adjusting the effective characteristic impedance through the amount of coupling, thereby maintaining the delicate balance between positive feedback and bandwidth extension.

The second feedback path of the proposed core is at the emitter side. It consists of the parallel connection of transmission line TLe1 and capacitor Ce1 (see Figure 2). This path provides negative feedback, which counteracts the strong positive feedback between base and collector (see Figure 4). The shunt capacitor Ce1 has a small impedance at the operating frequency, such that it barely affects the gain, while it still helps to stabilize the core at frequencies above 100 GHz. By combining the base–

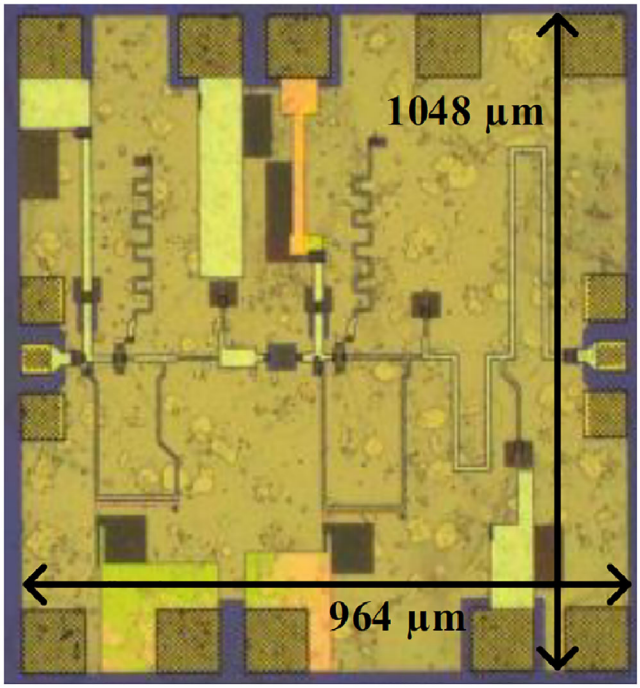

FIGURE 6 | Chip micrograph. Die size is 964 µm × 1048 µm.

collector and emitter feedback paths, stability and gain boosting can be achieved at the same time over a broad frequency range.

The gain of the first stage rolls off as frequency increases. In contrast, the second stage in Figure 4a exhibits a higher gain at high frequencies due to the negative resistance generated in the feedback path, which enhances the high-frequency response. As a result, the two stages complement each other gain roll-off, achieving an overall flat gain.

The transistor core inevitably exhibits conditional stability at some frequency range while pursuing broadband gain boosting. The conditional stability of the core can be properly controlled by placing both the source and load impedances far away from the unstable regions in the source and load stability circles. The losses from the interstage matching network further stabilize the core. After including the matching losses, the two-stage LNA becomes unconditionally stable (see the simulation results in Figure 7).

Figure 4a,b shows the maximum available/stable gain (G_{ma}/G_{msg}) of the transistor core of the second and the first stage, respectively. Both stages include the input shunt inductance utilized for the input matching (TLm in Figure 2). In the two stages, the transistor size for both the amplifying transistor Q1 and the varactor (V1) is 0.25×4 µm^2. The passive component values of the implemented first/second cores are as follows: C1 = 48/187.5 fF, Cf1 = 10/13.7 fF, Ce1 = 135 fF. The transmission line dimensions, expressed as (Z_0, electrical length), are as follows: TLm = (82, 117°)/(44, 18°), TLf1 = (82, 43°)/(82, 51°), TLf2 = (82, 54°)/(82, 56°), TLb1 = (62, 10°)/(62, 6°), TLc1 = (58, 15°)/(75, 24°), TLe1 = (82, 117.4°)/(82, 122°). The transmission line TLt1 has a length of 130 µm and is tunable from 53.3 to 65.3 pH by effectively modifying its characteristic impedance, corresponding to a tuning

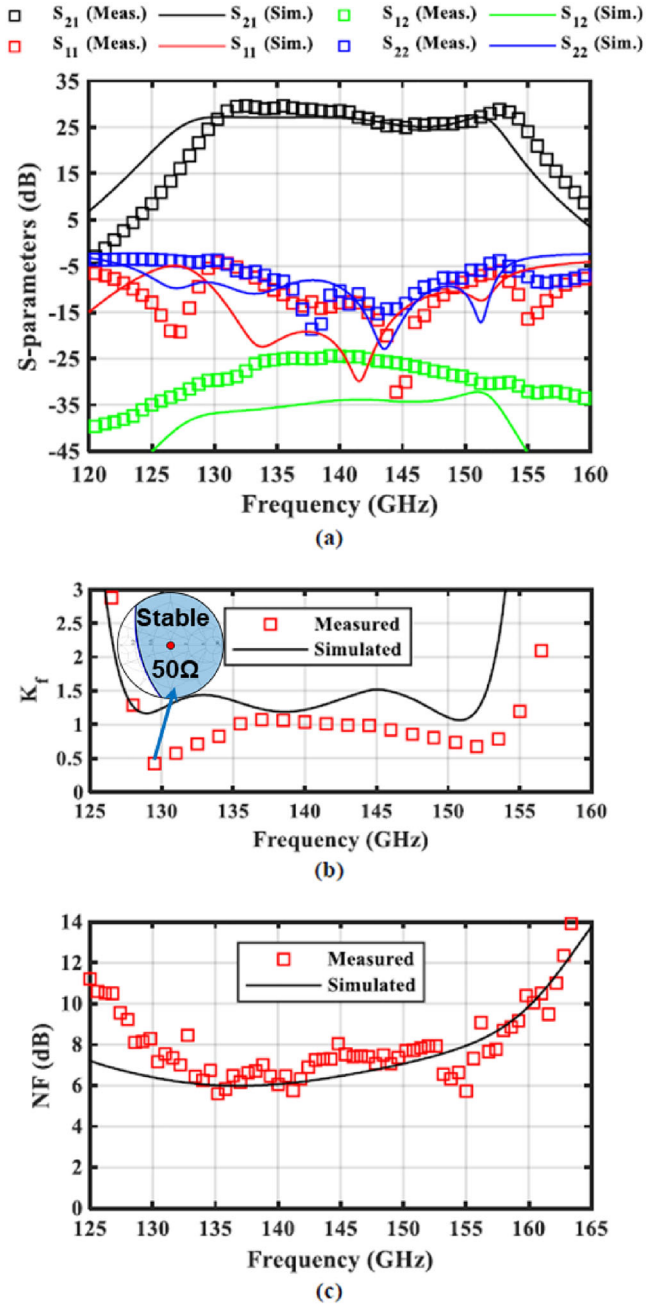

FIGURE 7 | Measurement results: (a) S-parameters, (b) stability factor (K_f) and (3) NF versus frequency.

range exceeding 20%. The LNA optimizes noise performance through the first stage and increases gain via the second stage by applying a slightly higher bias than the first stage. In the first stage, the circuit nearly satisfies the SNIM condition over a broad bandwidth. This is accomplished by finding TLb1 and TLc1 combinations, as described in [1, 4], along with additional passive components in the feedback path (Cf1, TLf1, TLt1, TLf2, TLe1, Ce1), enabling greater design flexibility to realize the broadband SNIM condition. Both the optimal noise admittance (Y_{opt}) and the conjugate of the input admittance (Y^*_{in}) closely approach a value of 50 Ω, which is equivalent to 0.02 Siemens (S) and 0 S for the real and imaginary part, respectively, as shown in Figure 5. This avoids the need for complex passives in the input matching network

TABLE 1 | D-band LNA performance comparison.

Reference	This work	[2]	[9]	[4]	[10]	[5]
Technology	250-nm InP DHBT	250-nm InP DHBT	45-nm RFSOI	65-nm CMOS	45-nm CMOS SOI	40-nm CMOS
f_{centre} (GHz)	142	130	138	152.2	150	153
BW (GHz)	25	20	7.4	11	25	24
NF (dB)	6.2	4∼6	4.3∼5.3	4.7	6.4	4.9
Gain (dB)	27	13	30.75	17.9	17.2	16.3
P_{DC} (mW)	2.5	11.2	25	13.7	30	16.1
OP1dB (dBm)	−9.9	−8.5[a]	−2.4	−6.9	—	—
FoM1[b]	64	21.5[a]∼27.4[a]	43.3∼46.5	28.1	22.3	29.7
FoM2[c]	−7.8	−19.6[a]∼−13.6[a]	−21[a]∼−17.8[a]	−19.5	—	—

[a]Simulated and estimated,

[b]$\text{FoM1} = 20 \times \log\left(\frac{\text{Gain}_{\text{lin}} \times \text{BW (GHz)}}{\text{P}_{\text{DC}}\,\text{(mW)} \times (\text{NF}_{\text{lin}} - 1)}\right)$.

[c]$\text{FoM2} = 20 \times \log\left(\frac{\text{Gain}_{\text{lin}} \times \text{BW (GHz)} \times \text{IP1dB (mW)}}{\text{P}_{\text{DC}}\,\text{(mW)} \times (\text{NF}_{\text{lin}} - 1)}\right)$.

between the GSG pads and the LNA, preventing degradation in noise and gain performance due to loss (see Figure 1). The second stage boosts the gain near G_{max} over a broad frequency range. Note that the long TL increases the value of U of the intrinsic transistor by 1 dB thanks to the negative resistance discussed in the previous section. The negative feedback of the emitter degeneration stabilizes the two cores as shown in Figure 4a,b. More specifically, the stability of the second stage around 160 GHz is especially affected (see Figure 4a).

While the first stage has a higher gain at lower frequencies, the second stage exhibits a higher gain at high frequencies, resulting in an overall flat gain over the frequency range of interest.

3 | Measurements

The chip, shown in Figure 6, is fabricated in a 250 nm InP DHBT technology. The S-parameters are measured with a Keysight network analyser (PNA-X) connected with VDI D-band extension modules and infinity probes. NF is measured with the gain method based on the downconverted output noise power. This setup includes a low-pass filter to suppress LO leakage to the network analyser.

The base–emitter voltages for the first and second stage are 755 and 800 mV, respectively. At the nominal supply voltage of 1 V, which has also been used in simulations, the measured gain is higher than the simulated value, due to a modelling mistake in the base–collector capacitance. While the circuit is stable at a 1 V supply, partially thanks to the tuning of the varactor, the supply voltage can be lowered to 770 mV, at which there is a better agreement with simulated S-parameters. At this supply voltage the DC power consumption is 2.5 mW. Although gate-bias tuning can affect stability, it was not adjusted further to avoid deviating from the design methodology and compromising consistency between analysis and measurement.

Figure 7a shows the S-parameter measurements at a 770 mV supply voltage: S21 equals 27 dB at 142 GHz with a 2.5 dB fluctuation between 130 and 155 GHz. Due to the high gain of the LNA, the input power for measuring S11 is set to -55 dBm, yielding slightly noisy measurement results. The peaks in the measured S11 and S22 have shifted compared to simulations. As a result, the gain peaks of the first and the second stage have shifted, yielding a shift of S21 with 3 GHz. For the same power consumption in measurements and simulations, the measured gain value is slightly higher than the simulated one. The higher gain, together with the increased S12 —possibly caused by substrate wave propagation from the output to the input and modelling mismatches —lead to a degraded stability. As shown in Figure 7b, the measured stability factor (K_f) exhibits dips at both low and high frequencies where $K_f < 1$, indicating conditional stability. This behaviour contrasts with the simulation, which exhibits unconditional stability across the entire frequency range. In the measurement, although the stability factor K_f drops below 1 at certain frequencies, the LNA maintains S_{11} and S_{22} below 0 dB and operates within a stable region of the source and load stability circle, as shown in Figure 7b, confirming stability in a 50 Ω system. The tunability of the chip can further stabilize the core at the cost of a slight gain reduction, fluctuation, and bandwidth shrinkage. A wider tuning range would be required to fully recover the performance variations observed in the measurements.

Figure 7c shows the measured NF. From 130 to 155 GHz, the minimum and maximum NF are 5.6 and 8.4 dB, respectively, which matches quite well with simulations. Further, the measured output 1-dB compression point (OP1dB) is −9.9 dBm at 142 GHz.

Table 1 compares this work to state-of-the-art D-band LNAs. This work consumes minimum DC power while achieving a high gain, low NF in broad bandwidth. Although the linearity (OP1dB) is lower than that of other LNAs, the proposed LNA still achieves the highest figures of merit, FoM1 (linearity-noninclusive) and FoM2 (linearity-inclusive), among the state-of-the-art D-band LNAs.

4 | Conclusions

This paper presents a two-stage SNIM LNA in 250-nm InP technology. Each stage uses a higher-order feedback network between base and collector, providing positive feedback, and negative feedback at the emitter to achieve both SNIM and gain boosting over a broad frequency range. The positive feedback relies on a long TL, providing a negative resistance. This compensates the loss from the embedding passives. Moreover, a part of the transmission line between base and collector is coupled with a varactor. While the loss of this varactor can be compensated by the negative resistance, it can be tuned to cope with process tolerances. The proposed LNA achieves a 27 dB gain and a 6.2 dB NF over a broad frequency range with an ultra-low DC power consumption of only 2.5 mW, resulting in the highest FoM among the reported D-band LNAs.

Author Contributions

Sehoon Park: conceptualization, formal analysis, writing – original draft. **Yang Zhang**: investigation, project administration, supervision, writing – review and editing. **Arno Hemelhof**: investigation. **Kristof Vaesen**: writing – review and editing. **Mark Ingels**: writing – review and editing. **Piet Wambacq**: methodology, project administration, supervision, writing – review and editing.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

Research data are not shared.

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