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Observation of fully recoverable leakage behaviour in HfO_2 gate oxide of WS_2 2D FETs induced by local mechanical stress

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Keywords: gate oxide, 2D TMDs, mechanical stress (MS), compressive stress, asymmetric structure, FET, leakage

Supplementary material for this article is available online

Abstract

A fully recoverable leakage behaviour is observed near the source side of two-dimensional (2D) back gate HfO_2 oxide field-effect transistors (FETs) when subjected to a gigapascal -level mechanical stress (MS) applied locally via a nanoindenter tip. Due to the asymmetrical device structure of 2D-FETs, the generated stress is distributed non-uniformly, with maximum compressive stress concentrated near the source 'S' terminal rather than the drain 'D' terminal. Among the studied channel lengths ($L \sim 0.135\ \mu$m to $L \sim 10\ \mu$m), longer channels exhibit higher stress near the source terminal than the drain side, attributed to proximity effects under a constant applied load. An increase in gate leakage current with increasing MS is consistently observed, suggesting the generation of shallow traps. At the same time, the apparent reduction in the band gap lower the barrier for electron emission, giving rise to behaviour that appears consistent with a low-voltage dependent Poole–Frenkel mechanism approaching ohmic characteristics. Notably, upon removal of the MS, the gate leakage fully recovers. These findings underscore the mechanical sensitivity of HfO_2 gate dielectrics in 2D TMDs semiconductor devices and provide new insights into MS-induced reliability concerns, as well as the potential for mechanically changed electronic responses.

1. Introduction

Gate oxide is a critical component determining the electrical performance and long-term reliability of field-effect transistors (FETs) [1], including emerging two-dimensional (2D) transition metal dichalcogenide (TMDs) FETs. Devices with 2D channels are drawing significant attention for logic applications. As interest in 2D materials continues to grow, mechanical stress (MS) has emerged as an effective tool for tuning their physical and electrical characteristics. Techniques such as substrate bending [2, 3], atomic force microscopy (AFM) nanoindentation—induced stress [4, 5], the blown-bubble bulge method [6], engineered substrate pillars [7], and induced wrinkling [8] have demonstrated notable changes in key characteristics, including bandgap modulation, mobility tuning, phonon behaviour, resistance, piezoelectric polarization, and shifts in Raman and photoluminescence (PL) spectra, as well as exciton-to-trion conversion.

Among these methods, AFM-based stress facilitates the application of stress locally in different sections of FETs to mimic locally generated stress during device fabrication and packaging. In contrast, other stress application methods induce stress globally throughout the layer. However, AFM-based stress is limited by the relatively low force application ($\sim\mu$N), which is significantly below the levels of MS ($\sim$GPa) typically encountered during fabrication, 3D integration, and packaging [9, 10]. Additionally, since 2D-TMDs layers are often located beneath

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passivation layers in our devices, such mechanical forces ($\sim\mu$N) are generally insufficient to induce stress beneath the oxide.

To induce stress at the $\sim$GPa level, a nanoindenter (NI) is a suitable tool for generating such high stress. The NI has previously been employed to study various semiconductor devices, including Ferroelectric RAM (FeRAM), 3D NAND, FinFETs, and silicon-based FETs [11–16], demonstrating a significant impact on their electrical characteristics. Therefore, understanding the influence of MS using NI on 2D FETs is also important. Notably, the 2D FETs employed have side contacts that land on the underlying gate oxide, offering better integration for industry-compatible devices. Therefore, in this context, the gate oxide beneath the 2D layer becomes a critical factor and needs further investigation.

In this work, we report the impact of MS on the leakage current through the HfO_2 bottom gate oxide in 2D FETs. The NI enables the application of locally applied $\sim$GPa-level stress using a 30 μm flat-end tip, offering insights into stress-induced degradation mechanisms. We systematically examine gate leakage behaviour under MS in 2D-TMD-based devices with varying channel lengths. Our results reveal a fully recoverable leakage response, underscoring the mechanical sensitivity of leakage currents and highlighting the importance of incorporating mechanical reliability considerations into the design and development of 2D FET semiconductor devices. The paper is organized as follows: section 2 describes the experimental methodology, section 3 presents the results and discussion, and section 4 concludes the study.

2. Experimental methodology

The study was conducted on fully back-gated WS_2-based n-type channel FETs, all with a width (W) of $\sim$1 μm, and Lengths (L) of 10 μm, 1 μm, and 0.135 μm. All devices were entirely fabricated in a 300 mm pilot line. The MOCVD WS_2 channel was grown directly on the Si wafer with the following back oxide stack: 10 nm TiN using PVD/10 nm ALD HfO_2/5 nm PEALD SiO_2. Afterwards, it was capped using Al_2O_3 seed layer, which enabled the atomic layer deposition of 10 nm HfO_2 layer. Side contact trenches were etched and filled with Ti/TiN/W, as shown in figure 1(b), which represents a TEM cross-sectional image of the device near the source (S) side, highlighting the back-gate oxide composed of SiO_2 and HfO_2 layers. The complete device under test (DUT) schematic is illustrated in figure 1(a). A modelled 30 μm diameter flat-end tip, covering the entire DUT, is also depicted in figure 1(a). Notably, the employed DUT features an asymmetric layout due to the gate structure's proximity to the drain contact, a factor that significantly influences the device's behaviour under applied MS.

To induce MS in the DUT by applying a vertical force, a Hysitron TI 950 NI equipped with a flat-end tip was positioned over the DUT. The indent location can be seen as the marked position in the optical image shown in figure 1(c). Since the NI lacks electrical characterization capabilities, electrical probes were placed on the metal pads within the setup, as illustrated in figure 1(c), to enable *in situ* electrical measurements. The electrical characteristics including transfer (I_D–V_G) and gate leakage (I_G–V_G) curves were measured using Keithley K2600 source-measure units. In this setup, the chuck served as the back gate (which was swept), the source (S) was grounded, and the drain (D) was biased at $V_D = +1$ V.

To study the effect of the vertically applied local force on the DUT's electrical characteristics, the applied force was incrementally increased from 100 mN to 900 mN using the NI tip. Electrical measurements were taken at each force level during three stages: before stress application (BS), during stress (DS), and after stress removal (AS), as schematically shown in figure 2. Since the stress induced in the DUT by the applied force could not be directly measured *in situ*, it was calibrated and estimated using finite element modelling (FEM) in Hexagon Marc software.

3. Results and discussion

The FET transfer characteristics were first measured without MS at $V_D = 1$ V, using varying channel lengths (10 μm, 1 μm, and 0.135 μm) and a constant width of approximately 1 μm, as the time-zero characteristics. Electrically stable behaviour was observed across all devices However, as the channel length is scaled down, there is a significant negative shift in the threshold voltage. This trend indicates greater n-type doping in devices with reduced channel length as shown in figure 3.

Now on upon applying incremental vertical force to the DUT using a NI, as described in the method shown in figure 2, the leakage through HfO_2 gate oxide into the source (S) terminal was observed beyond specific force thresholds. This leakage is evidenced by the source current—gate voltage ($I_S - V_G$) characteristics at $V_D = 1$ V, as shown for the $L \sim 1$ μm device in figure 4(a), where the I_S behaviour closely resembles the gate leakage current (I_G). The occurrence of this leakage at the 'S' terminal can be attributed to a higher MS observed at the 'S' terminal relative to the 'D', resulting from the asymmetric DUT layout (figure 1(a)). The increase in leakage current ($I_G - V_G$) from the source 'S' side with increasing vertical force is depicted in figures 4(b)–(d) for all channel lengths (L), with the onset of leakage (threshold force) occurring at different force levels for

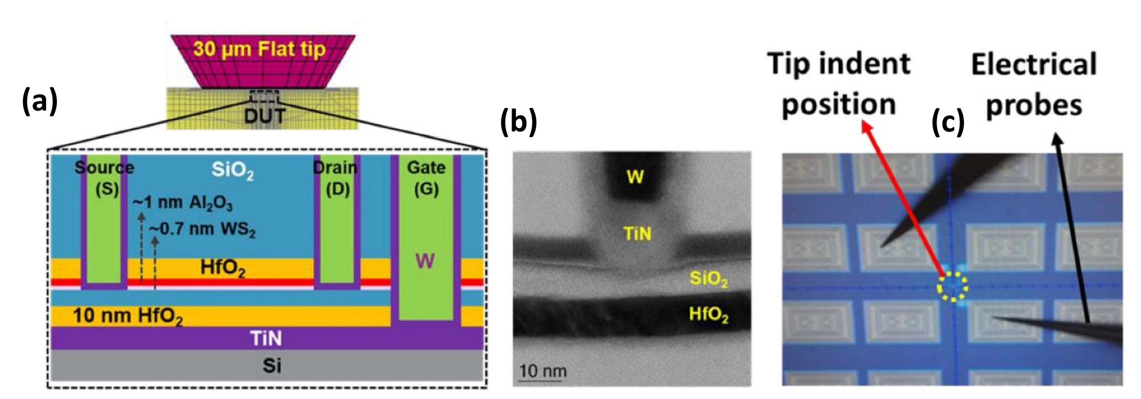

Figure 1. (a) Schematic of the DUT ($L \sim 10,1,0.135$ μm and $W \sim 1$ μm) with tip indentation which is zoomed in from the cross-sectional view of a 3D finite element model (FEM), which was used to convert the applied mechanical force to the generated mechanical stress (MS) in the devices for all the length cases, (b) cross-sectional TEM image of the device near the source contact, exhibiting distinct layers, and (c) DUT optical image with tip indent position mark and electrical probes.

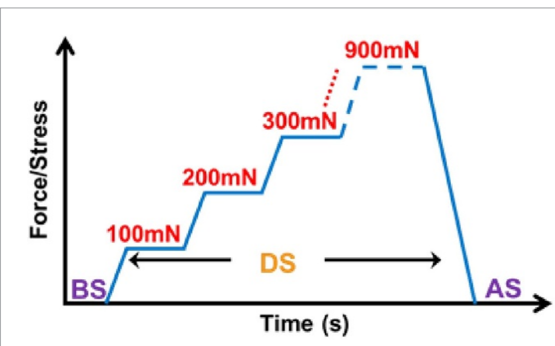

Figure 2. Schematic of the applied mechanical force/ stress method (BS: Before Stress, DS: During Stress, AS: After Stress) as a function of time over DUT.

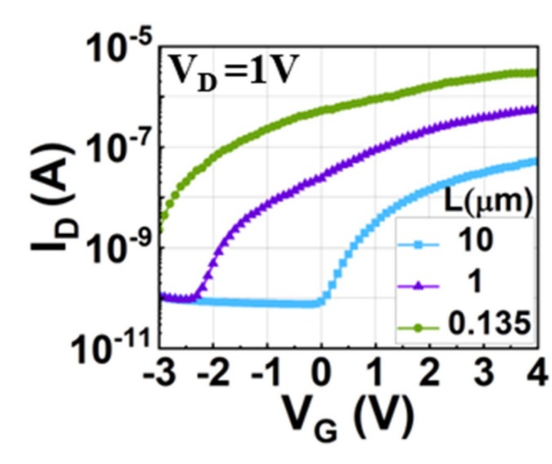

Figure 3. Transfer characteristics (I_D -V_G) of the device at $V_D = 1$ V, for different channel lengths 'L' with fixed width of 1 μm.

different 'L'. A similar trend of increased gate leakage under compressive stress has previously been reported for both SiO_2 and HfO_2, where the effect has been attributed to bandgap narrowing [17–19].

Importantly, the leakage current fully recovered following the removal of the applied force for all channels 'L', in our experiments, as shown in figures 4(b)–(d)), indicating that the observed effects were primarily due to the externally applied MS. To further confirm stability and leakage recoverability behaviour under adverse stress conditions, devices with different 'L' were continuously stressed for $\sim$1000 s at 900 mN. No change in leakage was observed for any channel length. Additionally, repeated tests involving 21 stress–release cycles at 900 mN demonstrated complete recoverability after each cycle, confirming excellent device stability. The details of the force application method and corresponding leakage characteristics are provided in the figures S1 and S2.

The devices also exhibited long-term leakage stability, as confirmed by measurements on the same stressed device re-tested after $\sim$2 years, which yielded similar leakage characteristics (figure S3). Furthermore, post-stress topographic scans revealed no plastic surface deformation (figure S4), and the WS_2 channel exhibited no significant modifications, as validated by PL and Raman spectroscopy (figure S5).

To further support our experimental findings, we performed mechanical FEM simulations using mechanical properties listed in table 1, and calculated the compressive stress generated throughout the device structure due to the applied tip load. The results exhibit non-uniform stress distribution, with the maximum compressive stress concentrated near the gate oxide of the 'S' terminal rather than the 'D' terminal. This asymmetrical vertical stress (S_{33} or S_{ZZ}) arises from the device design, as illustrated in figure 5, and corroborates with our experimentally observed leakage behaviour at the source side of the DUT. Given this, it becomes crucial to explicitly examine

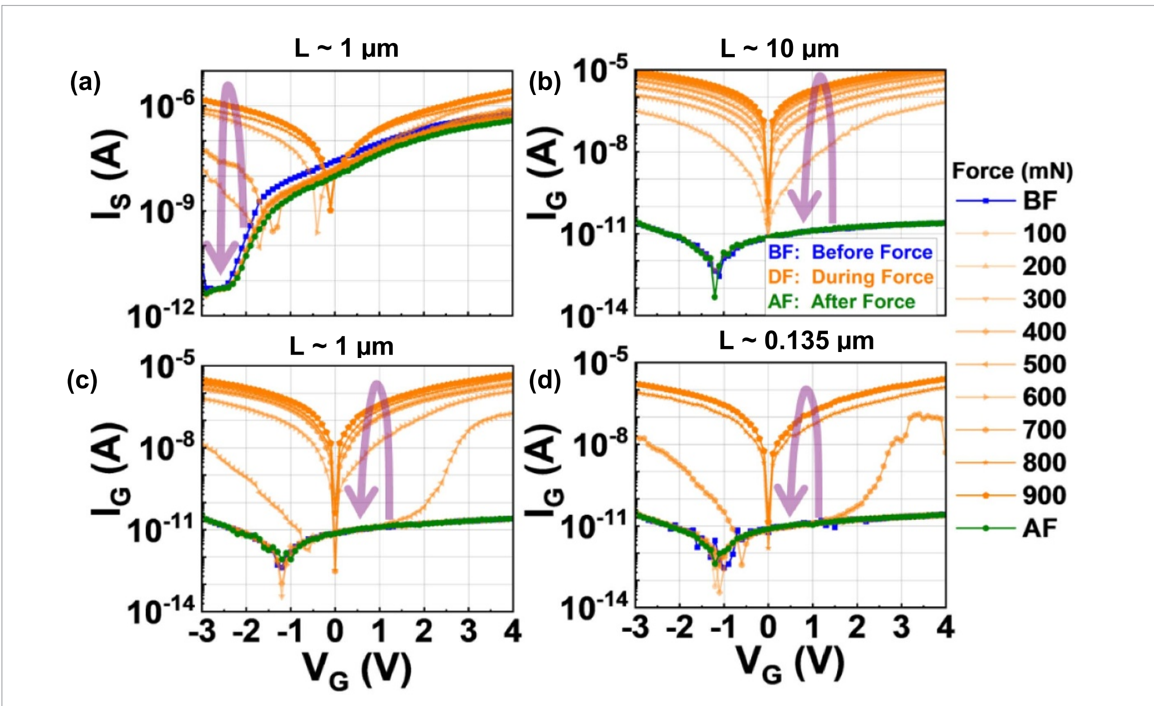

Figure 4. (a) I_S—V_G curves for channel $L \sim 1$ μm with $W \sim 1$ μm at $V_D = 1$ V. (b), (c), and (d) I_G—V_G curves for $L \sim 10$ μm, $L \sim 1$ μm, and $L \sim 0.135$ μm for before force (BF), during force (DF), and after force (AF), where BF and AF characteristics overlap indicating complete recovery.

Table 1. Material properties used in the FEM simulation.

Materials	Young modulus (GPa)	Poisson's ratio
WS_2	272	0.22
SiO_2	76	0.17
Si	169	0.26
HfO_2	222	0.25
TiN	290	0.36
W	405	0.28
Al_2O_3	380	0.24

the compressive stress generated in the gate oxide near the '*S*' and '*D*' terminal for three different channel '*L*', as obtained from the mechanical FEM simulations. The vertical stress distributions for each channel '*L*' are illustrated in the 3D contour map of stress at a 900 mN load, figures 6(a)–(c) for the '*S*' side and figures 6(d)–(f) for the '*D*' side. These stress maps clearly indicate that the highest compressive stress appears in the device with $L \sim 10$ μm, particularly on the '*S*' side, rather than in devices with shorter channels ($L \sim 1$ μm, 0.135 μm). This behaviour is attributed to the proximity effect between contacts, in devices with longer channels, the contacts are farther apart, so the tip-induced displacement causes localized stress at the contacts, resulting in greater stress buildup, particularly on the '*S*' side due to the structural asymmetry. In contrast, for shorter channel lengths ($L \sim 1$ μm and 0.135 μm), the closer proximity of the contacts causes the stress to be less isolated across the structure, leading to lower stress under the same applied load (900 mN). This trend is further validated by the stress values extracted from the FEM simulations over the oxide layer on the '*S*' side, derived from the reaction force applied by the 30 μm flat NI tip, as shown in figure 7.

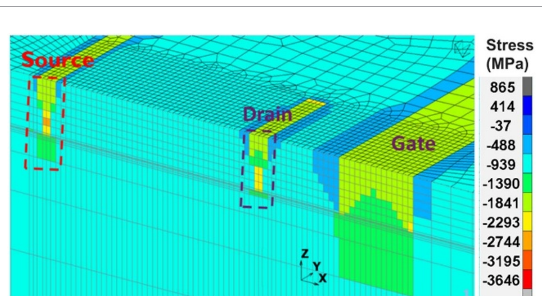

Figure 5. Stress distribution map from 3D-FEM simulation of the DUT ($L \sim 1$ μm, $W \sim 1$ μm) under a 900 mN vertical load, showing higher stress on the source side due to the asymmetric device layout.

This further allowed us to evaluate the observed leakage characteristics (I_G @ +1 V of V_G) for

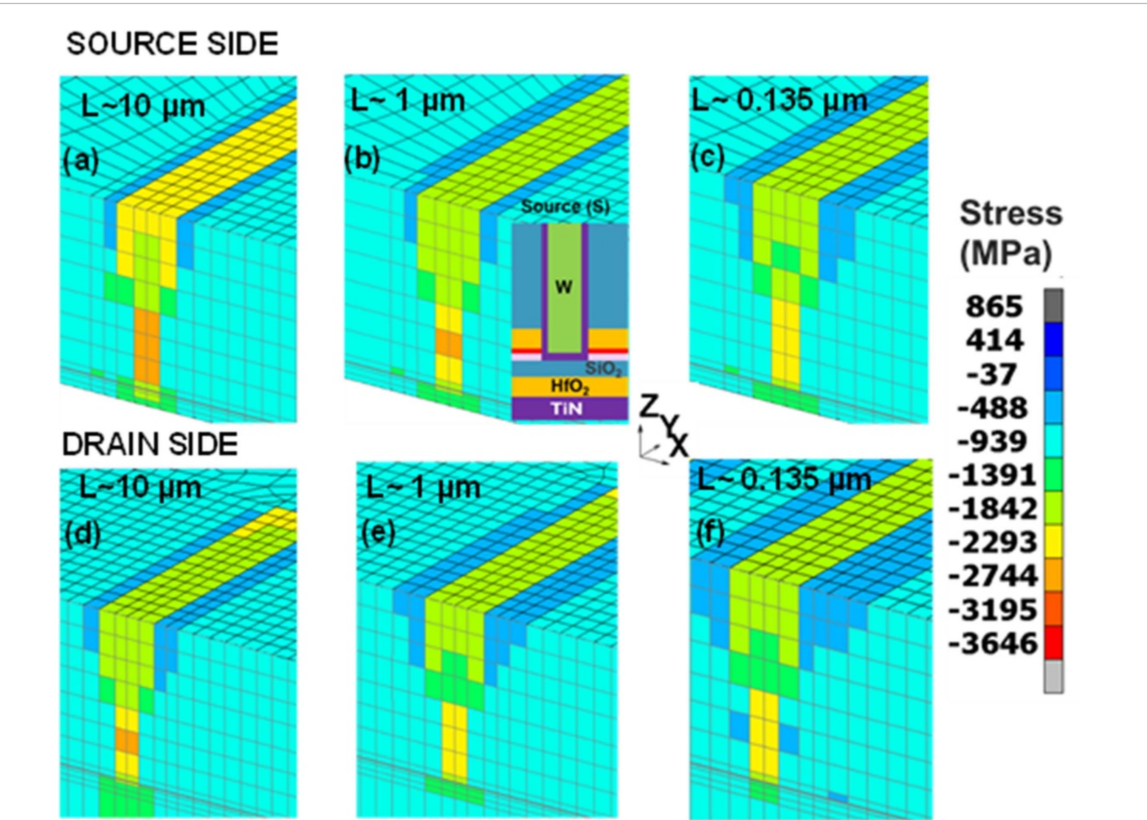

Figure 6. The stress distribution across the source ((a)–(c)) and drain ((d)–(f)) side for different channel lengths under a tip load of 900 mN was calculated using 3D mechanical FEM. The (a) and (d) is for $L \sim 10$ μm, where, maximum stress is observed near the source compared to the drain side, indicating a proximity effect between the contacts. (b), (c), (e), and (f) for $L \sim 1$ μm and $L \sim 0.135$ μm show lower stress values compared to $L \sim 10$ μm, as the closer proximity between contacts causes the stress to be less isolated, leading to lower stress under the same applied load (900 mN).

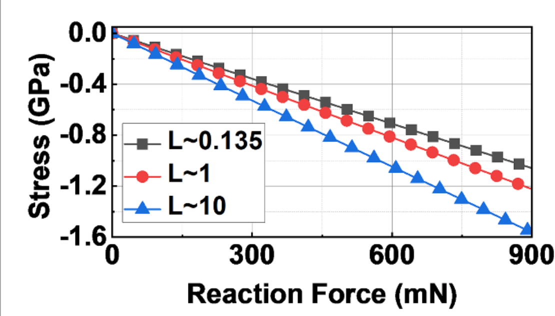

Figure 7. The FEM simulation converts the reaction force on the 30 μm flat tip maintained by the nanoindenter into a stress value (in the –z direction), over HfO_2 layer on the source side for different channel lengths.

calculated stress range. Measurements performed on 9 devices showed good uniformity, as evident from the statistical plots (figures 8(a)–(c)). For $L \sim 1$ and 0.135 μm devices, the leakage is observed at equivalent threshold stress values, while the $L \sim 10$ μm showed leakage at somewhat lower threshold value. Overall, the stress threshold ranged from ~ -0.4 to -0.8 GPa for different 'L' with complete recovery observed in all cases.

To investigate the leakage recovery behaviour and underlying conduction mechanisms, I_G–V_G data of

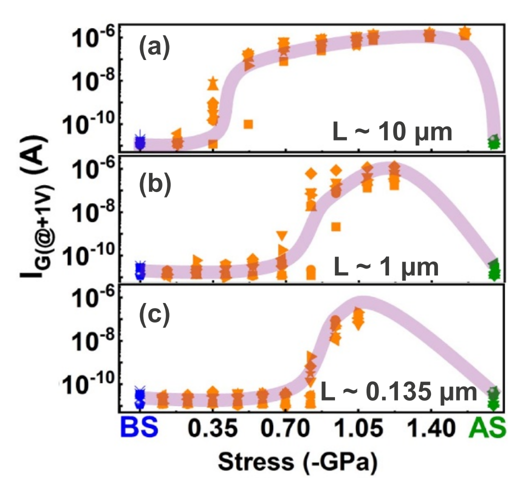

Figure 8. I_G (at +1 V) vs generated stress (GPa) for 9 devices in oxide under the source contact for three distinct devices with varying channel lengths; data in blue (before stress (BS), orange (during stress (DS), and green (after stress (AS)). Leakage behaviour is observed (a) for $L \sim 10$ μm after -0.35 GPa, (b) $L \sim 1$ μm after -0.8 GPa, and (c) $L \sim 0.135$ μm after -0.8 GPa.

$L \sim 10$ μm for different stress were analysed using different models. The Fowler–Nordheim (FN) tunnelling model showed no clear FN region (figure S6),

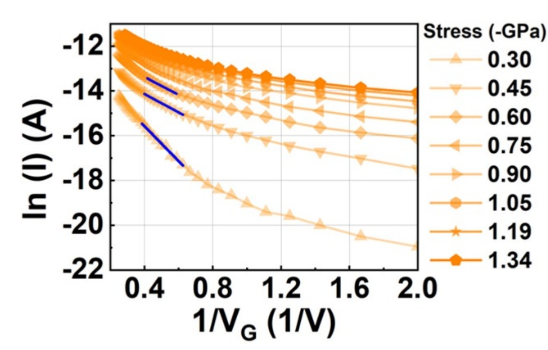

Figure 9. Trap assisted tunnelling (TAT) plot ((ln(I) vs $1/V_G$) of the gate leakage characteristics under incremental stress for a $10 \times 1\ \mu m^2$ device. The data can be fitted with a linear function in the medium voltage range up to 0.6 GPa of stress as shown by blue lines, suggesting that the TAT mechanism dominates in the low mechanical stress regime.

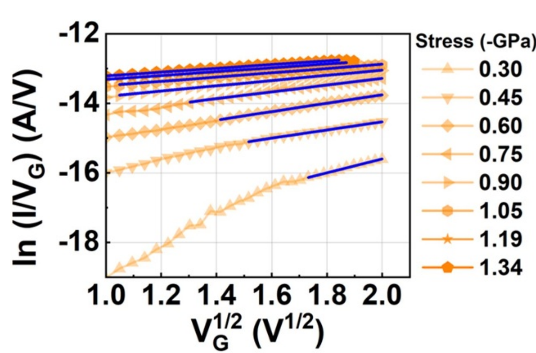

Figure 10. Poole Frenkel (PF) plot ((ln(I/V_G) vs $V_G^{0.5}$) of the gate leakage characteristics under incremental stress for a $10 \times 1\ \mu m^2$ device. A good linear fit is observed in the high-stress region and in the high-voltage range at lower stress as shown by blue lines, indicating that the PF mechanism is dominant in the device under these conditions.

suggesting that FN tunnelling is unlikely to be the dominant mechanism. Fits to the Quantum Point Contact model [20, 21] were also poor, suggest that this framework is not suitable for describing the observed conduction. The Trap Assisted Tunnelling (TAT) analysis (ln (I) vs $1/V_G$) [22, 23] exhibited linear behaviour in the mid-voltage range for 0.3–0.6 GPa stress (figure 9). Above 0.6 GPa, the linear behaviour region narrowed, suggesting that TAT is more relevant at intermediate voltages but becomes less significant under higher stress. From the TAT fits, the trap depth (Φ) below the HfO_2 conduction band was calculated and found to decrease from 0.32 eV to 0.20 eV as stress increased from 0.3 to 0.6 GPa. These values fall within the shallow-trap range reported for HfO_2 [24–27], indicating the possible generation of shallow traps. Furthermore, hysteresis measurements showed no measurable hysteresis (figure S7), indicating negligible contribution from deep traps [28].

The Poole Frenkel (PF) model (ln (I/V_G) vs $V_G^{0.5}$) [29, 30] provided further insight. From 0.3 GPa to 0.6 GPa, linear behaviour were obtained in the high-bias region, while at higher stresses (0.6–1.34 GPa) the linear range expanded with good agreement (figure 10). Increasing stress produced a decreasing PF slope, consistent with enhanced field-assisted lowering of the Coulombic barrier around charged traps. The trap depth extracted from the intercept also decreased with stress, reflecting a stress-induced reduction of the effective barrier height. Importantly, the change in trap depth ($\Delta\Phi$) obtained from both TAT and PF analysis (figure 11) showed close agreement, suggesting that both models probe the same stress-generated shallow traps and that PF conduction is a plausible pathway. Since no external stimuli were applied, the most likely cause for this enhanced barrier lowering is the externally applied MS, which has been reported to narrow the HfO_2 bandgap [18, 19]. This bandgap reduction decreases the separation

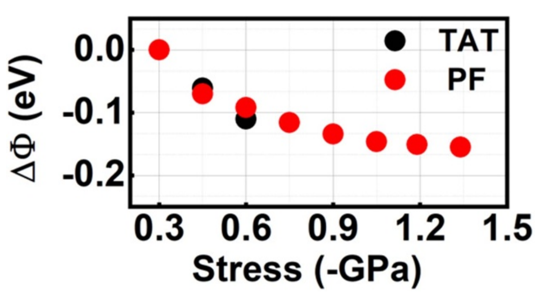

Figure 11. Change in trap depth ($\Delta\phi$) relative to 0.3 GPa extracted from both TAT and PF fits, showing close agreement between the trap depth from two mechanisms and supporting the proposed mechanism.

between trap levels and the conduction band edge, allowing electrons in shallow traps to escape more easily under an applied field.

The log-log plot generated for all channel 'L', as shown in figures 12(a)–(c) provides further support, where the power-law exponent (m) ($I_G \sim V_G{}^m$) of the I–V curve showed a continuous decrease toward near ohmic behaviour [31] (where, $m = 1$ represents purely ohmic behaviour) across different 'L' with increasing stress. The gradual transition toward ohmic behaviour suggests a progressive lowering of the energy barrier for electron emission due to stress-induced shallow trap formation and bandgap narrowing, making the PF conduction less voltage dependent. Furthermore, when the compressive stress is removed and the material structure returns to its relaxed state, the original energy barrier appears to be restored. Since the stress-generated traps are shallow, they are expected to have fast emission times, which will reduce leakage effectively and thereby explain the observed recoverability.

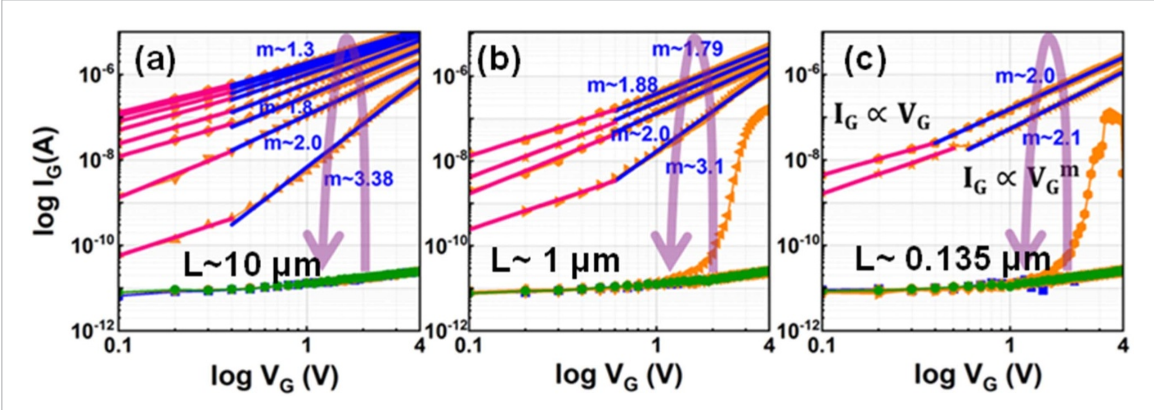

Figure 12. Log-Log plot for all channel lengths in BS, DS, and AS application. In (a), (b), and (c), the slope (m) gradually decreases toward ohmic behaviour with increasing MS leading to a stable leakage path and fully recovered I_G-V_G after stress.

4. Conclusion

The effects of external MS on 2D TMDs-based FET devices with varying channel lengths (L) were investigated, with a focus on the leakage characteristics through the bottom gate oxide. A fully recoverable leakage response was observed in HfO_2 gate oxide under ∼GPa-level MS applied over the source side, attributed to the asymmetric design of the DUT. This structural asymmetry causes maximum compressive stress to concentrate near the source terminal, particularly for devices with longer channel lengths, due to the proximity of the contacts, as confirmed by FEM simulations. A consistent increase in gate leakage current with increasing MS was observed, suggesting stress-induced shallow trap generation and a progressive reduction in trap energy, accompanied by possible bandgap narrowing. These effects appears consistent with PF conduction, which becomes progressively less voltage dependent, leading to a reduction in the I_G–V_G power-law exponent toward near-ohmic behaviour. Upon stress release, bandgap relaxation together with the expected fast emission times of shallow traps allow restoration of the original barrier, thereby supporting the observed recoverability of the device.

Data availability statement

The data cannot be made publicly available upon publication because they are not available in a format that is sufficiently accessible or reusable by other researchers. The data that support the findings of this study are available upon reasonable request from the authors.

Supplementary data 1 available at https://doi.org/10.1088/2053-1583/ae03d4/data1.

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