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ARTICLE

Reconfigurable Sequential-Logic-in-Memory Implementation Utilizing Ferroelectric Field-Effect Transistors

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ABSTRACT: In modern digital systems, sequential logic circuits store and process information over time, whereas combinational logic circuits process only the current inputs. Conventional sequential systems, however, are complex and energy-inefficient due to the separation of volatile and nonvolatile memory components. This study proposes a compact, nonvolatile, and reconfigurable van der Waals (vdW) ferroelectric field-effect transistor (FeFET)-based sequential logic-in-memory (S-LiM) unit that performs sequential logic operations in two nonvolatile states. Unlike conventional edge computing systems that require separate combinational logic circuits, sequential logic circuits (such as latches for short-term data storage), and nonvolatile memory for long-term data storage, this innovative S-LiM unit integrates logic and memory into a single nonvolatile vdW FeFET device. The nonvolatile ferroelectric elements directly replace both sequential logic and memory in conventional systems, eliminating frequent data transfers, reducing static power, and increasing the storage density. Six distinct logic operations are implemented in a single vdW FeFET through voltage-controlled ferroelectric polarization, highlighting the unit's reconfigurability. The device shows significant potential for low-power edge computing, especially where frequent power cycling is necessary. Its nonvolatile polarization retains the state without the need for storing processes, enabling rapid recovery at startup, even after extended power-off periods of tens of minutes. These features make the vdW FeFET-based S-LiM unit ideal for energy-efficient, high-density, and low-power edge computing, especially in remote operations with unstable power supplies. This innovation contributes to the development of next-generation, low-power electronics with enhanced efficiency and storage density.

KEYWORDS: *sequential-logic-in-memory, ferroelectric field-effect transistor, van der Waals ferroelectric materials, low-power edge-computing devices, in-memory computing*

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1. INTRODUCTION

In modern digital systems, sequential logic circuits are critical for temporary and local information storage, enabling sophisticated and synchronized data processing throughout the system, in alignment with the reference clock signal. Unlike combinational logic circuits, which process only current inputs to produce outputs, sequential logic circuits are required to store past input information as a state to process information over time. Their ability to retain state information facilitates the development of complex systems, making them crucial for applications such as microprocessors and communication systems.[1] Sequential logic can execute state-dependent operations by storing and utilizing past inputs and can facilitate essential tasks, such as synchronization, timing, and sequential execution. These functions are critical for the efficient operation of central processing units, registers, and counters.[2] Their integration is vital for managing complex processes and advancing modern computing and electronics. Conventional logic systems, primarily based on CMOS technology, are space-intensive due to separate components for combinational logic, sequential logic, and memory. Combinational gates (e.g., NOR and NAND) perform logic operations, while sequential elements (e.g., latches and flip-flops) serve as volatile memories for temporary data storage. If long-term data storage is required, then an external nonvolatile memory may be added to the system. Consequently, to operate such a logic circuit system, the integration of three distinct components — combinational logic circuits, volatile memory elements, and external nonvolatile memory — must be considered. This separation leads to a von Neumann

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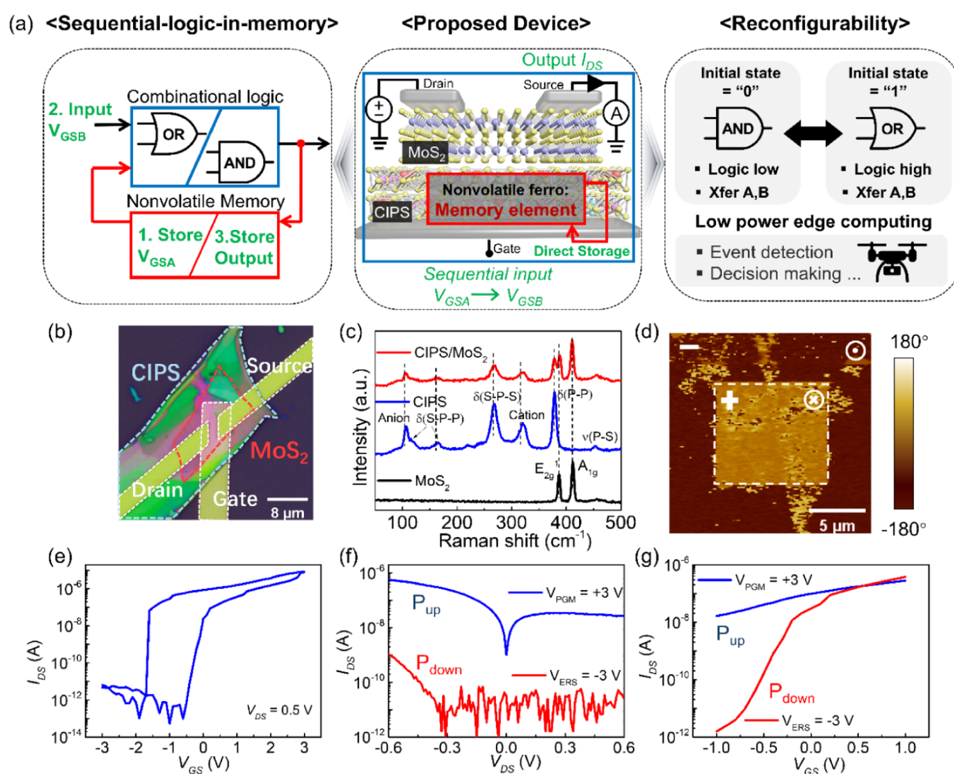

Figure 1. (a) Left: working concept of sequential-logic-in-memory; middle: vdW FeFET-based S-LiM unit: bottom-gated vdW ferroelectric field-effect transistor consisting of a ferroelectric dielectric CIPS and semiconductor MoS_2. Source and drain electrodes (10/80 nm Ti/Au) were deposited on the MoS_2 channel; right: reconfigurability and edge device/computing application. (b) Optical microscope image of a typical vdW FeFET. Colored dotted lines highlight the different components of the device. (c) Raman spectrum of the ferroelectric vdW device at room temperature. Bottom: MoS_2; middle: CIPS; top: CIPS/MoS_2 heterostructure. (d) PFM phase image scanned immediately after writing two square patterns with a size of 20 and 10 μm by applying −5 and +5 V voltages consecutively. (e) I_{DS}−V_{GS} curve of the vdW FeFET. (f,g) Output and transfer characteristics, respectively, for the vdW FeFET after applying program and erase voltage pulses (pulse width: 1 ms).

bottleneck due to the distinct processing and long-term memory units, resulting in data transfer and processing inefficiencies.

Recent advances in nonvolatile memory technologies have enabled the integration of sequential logic with nonvolatile elements, such as two-terminal memristors and three-terminal ferroelectric field-effect transistors (FeFETs), resulting in more compact, efficient circuits. Sequential logic in nonvolatile memory commonly uses two-terminal memristors, which operate based on resistive random-access memory, forming conductive channels via oxygen vacancies or metal clusters,[3−7] or through ferroelectric tunnel junctions.[8] Despite potential benefits, these devices face challenges: high leakage power due to low resistance, additional sensing circuitry to handle limited sense margins, high write power from current-based mechanisms, and large access transistors for write current. Furthermore, back-end integration can introduce parasitics that degrade the performance. Destructive read-out, where accessing data can alter or destroy stored information, complicates the design of sequential logic circuits, as it necessitates mechanisms to ensure data integrity during read operations. By contrast, FeFETs have emerged as promising nonvolatile memory candidates due to their electric-field-driven write operations, which avoid large write currents and improve energy efficiency. Additionally, FeFETs offer fast, reliable, and nondestructive read access through transistor amplification.[9] This combination makes FeFETs a major step forward in efficient, compact logic, and memory integration.[10]

Early implementations of nonvolatile sequential logic with FeFETs introduced nonvolatile latches and flip-flops, achieved by integrating FeFET backup modules with latches or replacing MOSFETs in conventional SRAM.[11−13] However, these designs still resemble traditional CMOS sequential logic, retaining challenges such as large area use and separation between logic and memory. Moreover, their CMOS-based design limits the reconfigurability. Subsequently, recent approaches have integrated sequential logic and nonvolatile memory components, introducing reconfigurability. For example, a reconfigurable sequential logic operation using HfO_2-based FeFETs with a pull-up device demonstrated NAND and NOR gates by applying specific source or back-bias voltages.[14] However, the number of achievable logic gates is limited. Zhang et al.[15] expanded sequential logic functions in a single FeFET by introducing interfacial charge trapping in HfO_2-based FeFETs, enabling eight Boolean functions. However, controlling the interfacial charge trapping is challenging and may lead to significant variation between devices, complicating the manufacturing process and reducing the overall reliability. Recently, significant advancements in van der Waals (vdW)-layered ferroelectrics have garnered interest owing to their exceptional performance characteristics, providing a breakthrough in addressing the limitations of ferroelectric oxide-based Fe-FETs.[16−24] Various categories of vdW ferroelectric materials have been explored, as well as several investigations on vdW FeFETs incorporating excellent nonvolatile memory capabilities.[25−31] However, for logic-in-

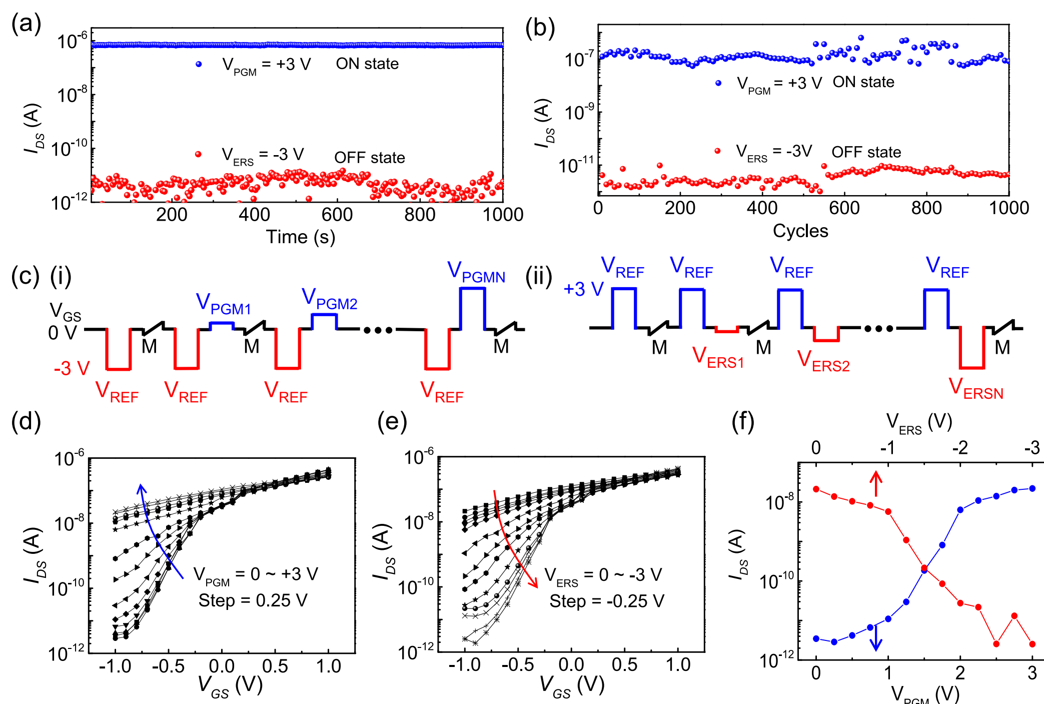

Figure 2. (a) Retention of the memory states after applying positive programming and negative erasing voltage pulses, measured at $V_{GS} = -1$ V and $V_{DS} = 0.5$ V. (b) Endurance of the memory states. (c) Diagrams showing the sequential test procedures. (d, e) I_{DS}–V_{GS} curves for the forward (d) and reverse (e) V_{GS} step direction. The maximum amplitude of V_{GS} was 3 V, and the V_{GS} step was 0.25 V. V_{DS} was 0.5 V. The pulse width was 1 ms. (f) I_{DS} values of the device as a function of the program (blue line) and erase (red line) pulse amplitudes, extracted from panels d and e at $V_{GS} = -1$ V.

memory applications, vdW heterostructure devices are limited to combinational logic[32,33] where the output is purely a function of the current input, lacking any ability to store or reference historical input data.

This study introduces a novel vdW FeFET-based sequential logic-in-memory (S-LiM) unit that integrates compact, nonvolatile, and reconfigurable sequential logic gates into a single device. The design replaces volatile memory in conventional circuits with nonvolatile vdW ferroelectric material, eliminating the need for external nonvolatile memory (NVM) and reducing energy consumption. This eliminates the need for external nonvolatile memory (NVM) and separate memory components, significantly reducing energy costs and creating a more efficient and streamlined system. The fabricated vdW FeFET demonstrates excellent performance, including a high on/off ratio of 10^5, endurance of $>10^3$ cycles, and stable retention of $>10^3$ s. The device stores the outcome of the first signal stimulus via persistent ferroelectric polarization, enabling subsequent logic operations without data transfer. This integration improves efficiency and supports intermittent power operation with rapid recovery. Using voltage-controlled ferroelectric polarization, the device performs six distinct reconfigurable sequential logic gates. When the initial state is set to a high-resistance state (HRS), the device can perform Logic Low, Transfer A, Transfer B, and AND logical operations. These logical operations can be reconfigured to perform other logical operations, including Logic High and OR, when the initial state is set to a low-resistance state (LRS). Furthermore, the potential of the vdW FeFET-based S-LiM unit for energy-efficient and high-performance Internet of things (IoT) edge-computing devices is demonstrated. In addition to improving the computational efficiency, the proposed circuit can quickly recover and start up without data transfer between the nonvolatile storage and processing circuits for state restoration when the supply voltage is reapplied. The power-off interval could be extended to tens of minutes, demonstrating the flexibility and wide applicability of the device. The vdW FeFET-based S-LiM unit can enhance the energy efficiency and performance of IoT edge computing devices, offering a streamlined and versatile solution for modern computing needs.

2. RESULTS AND DISCUSSION

2.1. Working Principle and Performances of the VdW FeFET-Based S-LiM Unit. The operational scheme for a compact, nonvolatile, and reconfigurable vdW FeFET-based S-LiM unit capable of performing sequential logic operations in two nonvolatile states is illustrated in Figure 1a. The schematic on the left in Figure 1a shows the S-LiM operation of the proposed vdW FeFET, which integrates reconfigurable logic operations with an NVM element. Initially, the previous information is stored in the NVM element as a state (step (1): storage of the first input signal V_{GSA}), and this state determines the type of logic operation applied to the current input (step (2): application of the second input signal V_{GSB}). The result of the logic operation is stored directly in the NVM (step (3)). This process is streamlined in a single vdW FeFET, as shown in the middle of Figure 1a. By contrast, as illustrated in Figure S1a, conventional CMOS-based sequential logic circuits separate memory elements (such as latches) from the logic operation circuit, each consisting of four to six transistors in this example. This separation necessitates data transfer between the computing and storage components for each operation. Additionally, an external NVM is required for long-term data storage through power cycles, resulting in area/static power consumption and substantial data transfer overheads.

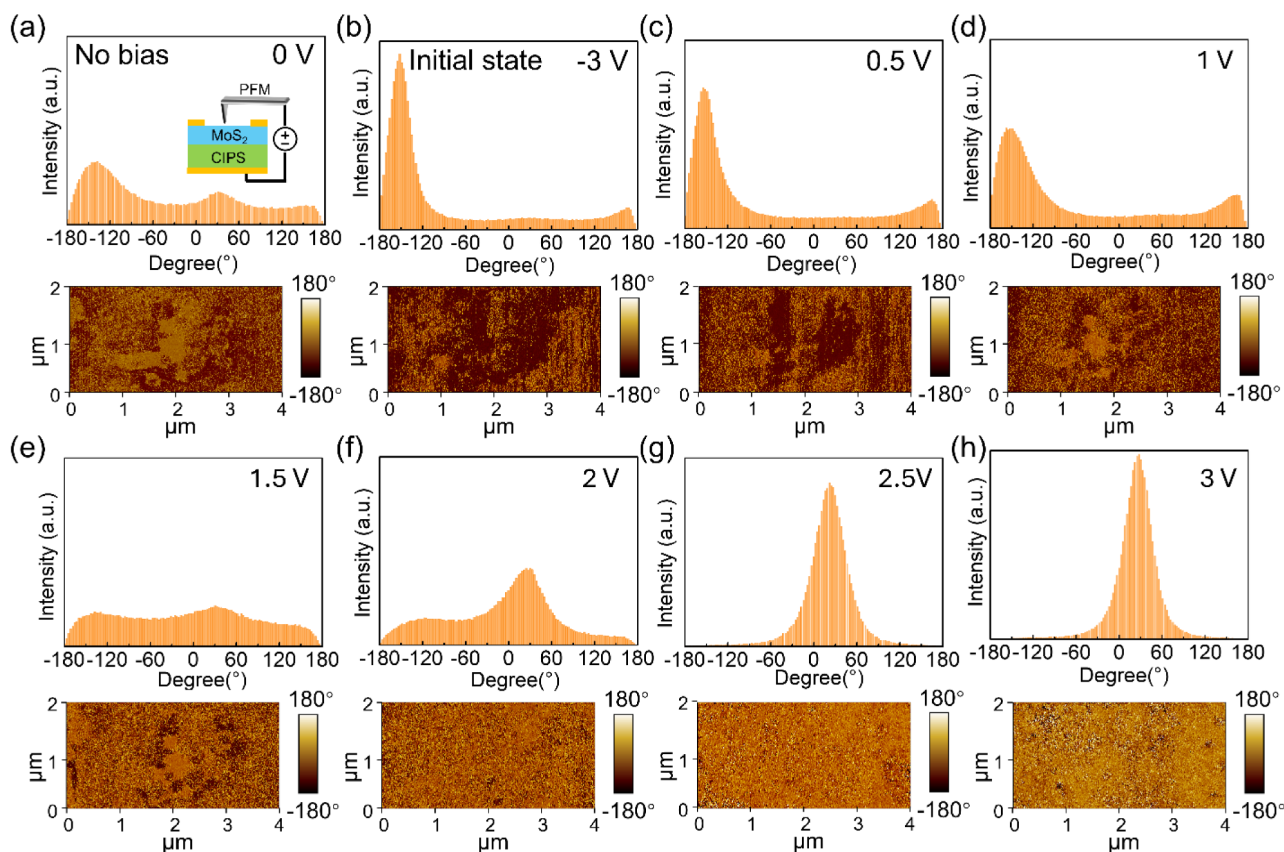

Figure 3. (a−h) PFM scanning of the vdW FeFET channel area with varied external voltages. For each part, the top shows the degree distribution of polarization, while the bottom presents the corresponding phase images of the scanned area. (a) Fresh state. (b) Initial state (initialized by a voltage of −3 V). (c−h) Applied voltage changed from 0.5 to 3 V in steps of 0.5 V.

The proposed vdW FeFET-based S-LiM device, as shown in the middle of Figure 1a, utilizes few-layer vdW semiconductor MoS_2 as the channel and ferroelectric $CuInP_2S_6$ (CIPS) as the gate dielectric. The source and drain electrodes are placed at both ends of the MoS_2, and the bottom gate applies sequential voltage pulses, with the drain current serving as the logical output. The device retains the previous state directly as the degree and/or direction of polarization of the CIPS and can wait for the next input signal, even without a continuous power supply. When the second input is applied, the logical output is stored immediately after each operation. The voltage-controlled ferroelectric polarization allows the device to support up to six different logic functions by altering its initial state, as demonstrated experimentally in Figures 2−4. The reduced footprint, versatile logic operations, and low static power render the vdW FeFET well-suited for low-power edge-computing nodes, which often operate in environments with unstable power supplies and low activity until specific triggers occur (as shown in Figure 5).

Figure 1b shows an optical microscopy (OM) image of the fabricated MoS_2−CIPS heterostructured vdW FeFET, with the colored dotted lines highlighting the device components. The Au bottom gate was first deposited by using electron-beam evaporation. Thin flakes of CIPS and MoS_2 were then sequentially stacked, aligning with the bottom gate. Source and drain electrodes (10 nm Ti/80 nm Au) were deposited onto the two ends of the MoS_2 flake, featuring a channel length of 2 μm and a width of 4 μm. Atomic force microscopy (AFM) characterization of the vdW FeFET, showcased in Figure S2, determined the thicknesses of MoS_2 and CIPS flakes as approximately 3.5 and 150 nm, respectively. In Figure 1c, the mechanically exfoliated vdW MoS_2 and CIPS flakes, as well as their heterostructures, were confirmed by Raman spectra, exhibiting peaks that align well with previous reports on MoS_2 and CIPS.[25,29] No noticeable Raman shift was observed in the heterostructure, indicating a high-quality interface between the materials. Piezoresponse force microscopy (PFM) was conducted to verify the out-of-plane (OOP) ferroelectricity and polarization switching in CIPS (Figure 1d). The phase was acquired immediately after consecutive writing of two square patterns with opposite tip bias (−5 and +5 V), demonstrating that the polarization direction can be reversed by external bias. The topographic and amplitude images, detailed measurement setup of the PFM, and hysteresis loop are shown in Figure S3. The polarization versus electric field (P−E) hysteresis loop is shown in Figure S4.

Figure 1e shows the I_{DS}−V_{GS} characteristics of the vdW FeFET device. In the bidirectional scanning mode, the gate voltage (V_{GS}) varied from −3 to +3 V and then back to −3 V, while the consistent drain voltage (V_{DS}) was 0.5 V. The vdW FeFET displayed a characteristic anticlockwise hysteresis due to ferroelectric polarization switching, with a hysteresis window of 2 V and a high on/off current ratio of 10^7. The observed low subthreshold change of 22 mV/dec over five decades of drain current may be attributed to the negative capacitance effect of CIPS under optimal capacitance matching conditions between the ferroelectric dielectric and the channel.[32,34] The gate current measured below 10^{-10} A (Figure S5a) ensured a high input impedance for the logic gate circuits. The output characteristic curve of the vdW FeFET is shown in

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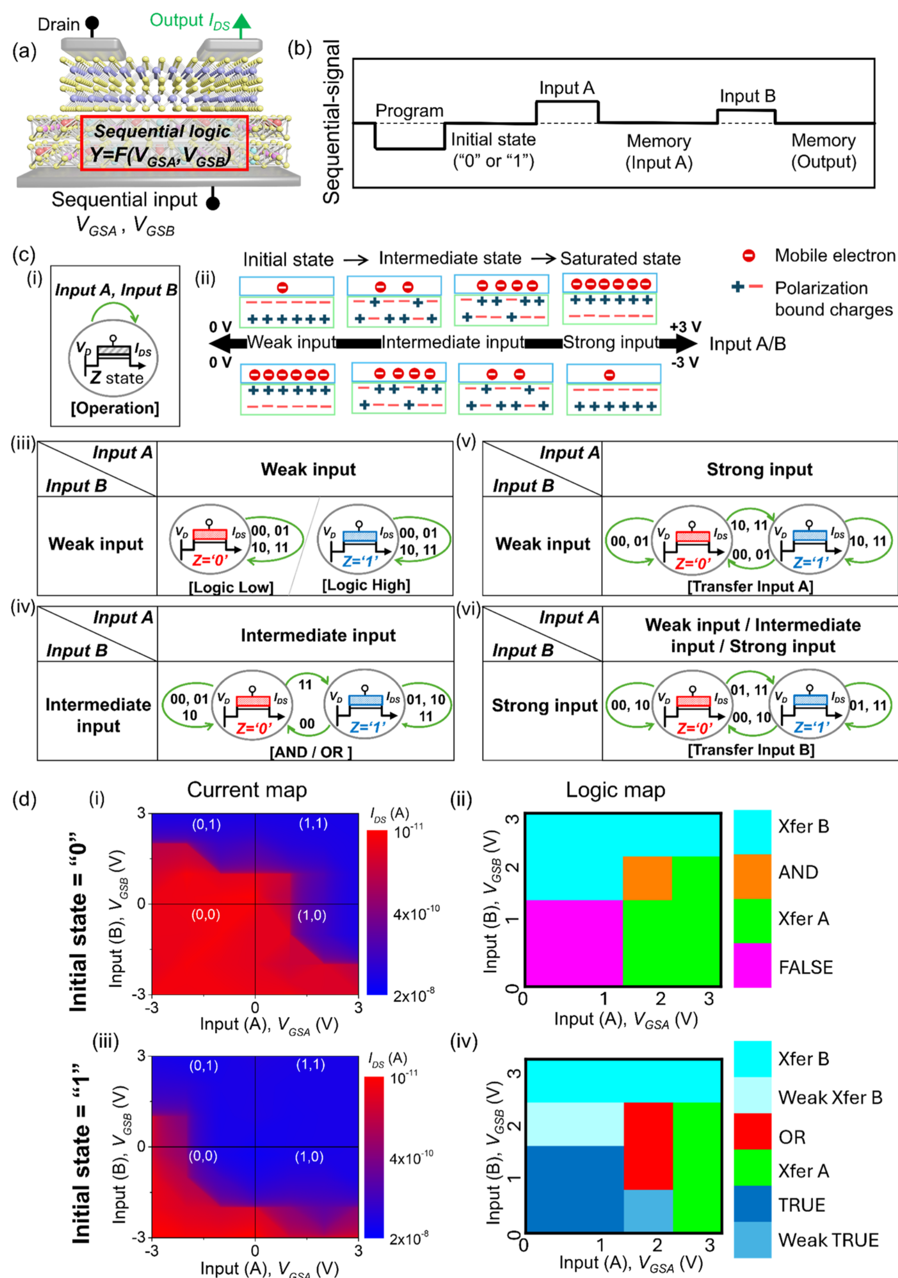

Figure 4. (a) Schematic of the concept of a reconfigurable S-LiM. (b) Schematic of the sequence-signal adopted to achieve reconfigurable logic operations. (c) (i) Schematic of the device operating method, Z represents the state of the device; (ii) schematic demonstration of resistance evolution of the MoS_2 channel caused by continuous electrical signal stimulation-induced polarization change (up: polarization direction transits from downward to upward; down: polarization direction transits from upward to downward); (iii–vi) schematic FSM representation of the vdW FeFET-based S-LiM unit and the optimized condition for each logic operation. (d) I_{DS} mapping as a function of the two sequential stimuli (i.e., first voltage pulse (input A) and the second voltage pulse (input B)) when the device is preprogrammed to state "0" (i) or state "1" (iii). The corresponding logical operation distribution under different input A and B amplitudes when the device initial state is "0" (ii) or "1" (iv).

Figure S5b, while the transfer curves for different V_{GS} sweep ranges are presented in Figure S6a. The HRS and LRS of the device were evident in the $I_{DS}-V_{DS}$ (Figure 1f) and $I_{DS}-V_{GS}$ (Figure 1g) curves after removing the positive and negative 3 V programming and erasing pulses (V_{PGM} and V_{ERS}, respectively; pulse width = 1 ms). In Figure 1f, $I_{DS}-V_{DS}$ was measured in a small V_{DS} (−0.6 to 0.6 V) range with a fixed V_{GS} = −1 V and two clear resistance states with a ratio of >10^4 were obtained. The asymmetric output curve in Figure 1f likely arises from nonuniform polarization switching across the gate area, which resulted in localized variations in the electric field along the channel. For the $I_{DS}-V_{GS}$ curve in Figure 1g, the V_{GS} range was from −1 to 1 V and V_{DS} was constant at 0.5 V, and a resistance state ratio >10^4 was also obtained when V_{GS} was −1 V. The operating principle of the MoS_2−CIPS FeFET is illustrated by the energy band diagrams for the P_{down} and P_{up} states (Figure S7). In the P_{down} state (Figure S7a), the negatively bound charges at the CIPS top surface depleted the electrons in the channel, resulting in an HRS. Conversely, in the P_{up} state (Figure S7b), positively bound charges at the CIPS top surface

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induced electron accumulation, leading to an LRS. The substantial resistance changes with polarization reversal allowed these states to represent ″0″ and ″1″ in digital circuits, thus enhancing circuit tolerance. The performance comparison with other reported vdW FeFET NVM is shown in Table S2.

The stabilities of the LRS (program state) and HRS (erase state) of vdW FeFET were further confirmed. A retention test was performed on the device after removing a 1 ms gate voltage pulse of ±3 V (Figure 2a), demonstrating that the two stable resistance states maintained a sufficient difference without degradation for over 10^3 s. A cyclic endurance test under variation of the program and erase state cycles was performed (Figure 2b), which demonstrated the stability of the LRS and HRS over 10^3 cycles. These results demonstrate the feasibility of the device as an S-LiM computing medium.[35]

More specific measurements that adopted multiple-step voltage pulse stimulation were conducted (Figure 2c−f). Figure 2c illustrates the sequential test procedure. As shown in Figure 2c(i), a −3 V erase pulse (V_{REF}) was initially applied to set the reference state of the device. The transfer characteristic was then measured with V_{GS} varying from −1 to 1 V (labeled as M in Figure 2c(i)) to determine the current state. Subsequently, a series of increasing positive program pulses (V_{PGM}, from V_{PGM1} to V_{PGMN}) ranging from 0 to 3 V in 0.25 V steps was applied following a V_{REF} erase pulse. The transfer characteristics were measured immediately after each V_{REF} and V_{PGM} pulse pair. Figure 2c(ii) illustrates the reverse procedure using 3 V V_{REF} and a series of negative program pulses (V_{ERS}, from V_{ERS1} to V_{ERSN}). The resulting transfer curves are shown in Figure 2d,e. Figure 2d demonstrates that, after applying −3 V V_{REF}, the current showed three distinct stages with increasing V_{PGM}: initially low, then increasing, and finally saturating. Figure 2e shows the reverse process with 3 V V_{REF} and negative V_{RES} pulses, where the current also showed three stages: initially high, then decreasing, and finally saturating. To illustrate the voltage boundaries of these stages more clearly, the I_{DS} values of the device as a function of the program (blue) and erase (red) pulses were extracted from Figure 2d,e at V_{GS} = −1 V (as shown in Figure 2f). For the program pulses (V_{PGM}), the current remained low when $V_{PGM} < 1$ V, increased between 1 and 1.75 V, and saturated at $V_{PGM} > 1.75$ V, stabilizing in a low resistance state. For the erase pulses (V_{RES}), the current remained high when V_{RES} was >−1 V, decreased between −1 and −2.25 V, and saturated at $V_{RES} < -2.25$ V, stabilizing in a high resistance state.

2.2. Voltage-Controlled Ferroelectric Polarization. The current changes in response to the voltage are linked to the ferroelectric polarization properties, which are controlled by an external electric field. To directly observe the voltage-controlled ferroelectric polarization, PFM measurements were conducted in the channel area of the vdW FeFET, as shown in Figure 3. This voltage-controlled ferroelectric polarization accounts for the current changes shown in Figure 2d−f, as it influences the channel's electrostatic potential and modifies the channel current. The polarization state was visualized using the PFM phase distribution (top of Figure 3a−h), while the bottom images show the corresponding PFM scans. Initially, without any external voltage, the PFM scan revealed that the dipoles in the CIPS were partially aligned downward and partially upward (Figure 3a). Applying a −3 V voltage between the gate terminal and the PFM tip (0 V) initialized the polarization, resulting in a predominant PFM phase of approximately −150 degrees, indicating downward alignment of the dipoles (Figure 3b). Consequently, with this saturated downward polarization, electrons in the MoS_2 channel were depleted, leading to a minimum level of channel conductivity. Subsequent PFM imaging was performed with gate voltages ranging from 0.5 to 3 V in 0.5 V increments, with the PFM tip held at 0 V, to observe the voltage-controlled ferroelectric polarization. At 0.5 V (below the coercive voltage, Vc, as described in Figure S4), the dipoles remained predominantly upward (Figure 3c). As a result, the channel's electrostatic potential did not change significantly, and the channel current also remained low. At 1 V, near Vc, some dipoles began to reverse (Figure 3d), but without enough reversed ferroelectric dipoles, the current did not change significantly (Figure 2e,f). Additionally, when the transfer curve sweep range was set between −1 and 1 V, no hysteresis was observed (Figure S6a). At 1.5 V (Figure 3e), which exceeds Vc, dipole switching commenced, achieving an equilibrium in which approximately 50% of the dipoles were polarized upward and 50% downward. At this stage, the channel current began to increase, although the change was not yet substantial. As the voltage increased further, more dipoles flipped to an upward orientation (Figure 3f−h). As the polarization continued to evolve, the enhancement in current became more noticeable, although it did not yet reach the saturated state. At 2.5 and 3 V, the PFM phase distribution spiked to 30°, with all ferroelectric dipoles aligned upward (Figure 3g,h), leading to the highest current levels observed. The corresponding process of channel current change can be found in Figure 2d,f. The reverse voltage control process, which involves switching polarization from upward to downward, was also tested and is presented in Figure S8.

2.3. Reconfigurable S-LiM. Those results demonstrate that the polarization inversion in the vdW FeFET can be regulated by varying the external voltage, thus demonstrating the tunability of the ferroelectric response. OOP polarization in the device ensures long-term retention of the initial state of the signal, allowing it to be preserved even after the signal is removed, which influences subsequent logic operations. Logic outputs are stored directly after execution with the voltage-controlled ferroelectric polarization of the CIPS, enabling the adjustment of the program and erasing voltages to control polarization inversion. Building on these capabilities, we further demonstrated that the reconfigurable S-LiM functionality of the device was further demonstrated. Figure 4a presents a schematic of the reconfigurable S-LiM concept, in which sequential input signals V_{GSA} and V_{GSB} are applied at the gate terminal. The logic output is stored via the polarization of CIPS and represented by I_{DS}. Figure 4b shows how sequential input signals enable reconfigurable S-LiM operations by using a vdW FeFET-based device. The process begins with an initial program or erase pulse to set the starting state. Next, the first input signal, "A," is applied, and once deactivated, the resulting state is stored. The next input, "B," is then applied, and the final logic output, derived from both inputs A and B, is promptly stored in the device. The operating scheme can be visualized with the state transition diagrams as shown in Figure 4c, and their legend is shown in Figure 4c(i), where "Z″ indicates the resistance state of the device, with "1" representing an LRS and "0" representing a HRS. The curved arrow highlights the transition in the resistance state due to inputs A and B, where positive signals are encoded as logical "1" and negative signals as logical "0." Figure 4c(ii) shows the

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polarization response to the voltage steps with positive and negative voltages in the top and bottom rows, respectively. As shown in Figures 2 and 3, the polarization (or resistance) state progresses through three phases: no change, intermediate change, and saturated change. Figure 4c(iii) shows the conditions for each logic operation and presents a schematic finite-state machine (FSM) for the S-LiM unit, corresponding to the operations in Figure 4c(i). When both inputs A and B are below the coercive voltage (Vc) and do not trigger polarization changes (weak inputs), the current remains unchanged, resulting in either a Logic Low or Logic High (Figure 4c(iii)). As shown in Figure 4c(iv), if inputs A and B exceed Vc and cause intermediate polarization changes (intermediate inputs), only two positive inputs can shift the HRS (initialized with a −3 V pulse) of the device to an LRS, acting as an AND gate. Conversely, only two negative inputs can change the LRS (initialized with a 3 V pulse) of the device to an HRS, enabling the OR gate functionality. Figure 4c(v,vi) shows the logical operations for Xfers A and B, respectively. The sequential nature of the inputs is crucial. When input B is the second signal and has a sufficient amplitude to induce saturated polarization (strong input), it overrides the effect of input A, causing the logic output to follow the polarity of input B (Xfer B operation). However, if the amplitude of input B is insufficient to induce polarization (intermediate input) and input A is sufficiently large to reach saturated polarization, then the logic output follows input A (Xfer A operation). This design highlights the versatility and efficiency of the reconfigurable S-LiM unit for executing multiple logic operations in a compact device architecture.

To verify the implementation of these logic gates, I_{DS} values were collected for various combinations of V_{GSA} (input A) and V_{GSB} (input B) at V_{DS} = 0.5 V and V_{GS} = −1 V, as shown in Figure 4d(i) (initial state ″0″) and (ii) (initial state ″1″). Both V_{GSA} and V_{GSB} values varied between −3 and 3 V. Figure 4d(ii,iv) displays logic maps generated from the current distributions shown in Figure 4d(i,iii), respectively, based on a threshold current (I_{th}) of 5×10^{-5} A. In these maps, I_{DS} values > I_{th} were encoded as logical ″1,″ while those <I_{th} were encoded as logical ″0.″ A 50% margin around I_{th} was applied to enhance the reliability of the logic operations. I_{DS} values falling outside this margin indicate “strong” logic operations, while those within the margin are considered “weak.” These logic maps show how the reconfigurable sequential logic gates are distributed across different V_{GSA} and V_{GSB} amplitude combinations, aligned with the expected behaviors outlined in Figure 4c. The Logic Low and Logic High gates clustered at the lower left of the two maps, indicating input amplitudes that were too small to cause significant polarization changes. The AND and OR gates were centered on the map, where the input signals resulted in unsaturated polarization changes. The Xfer A gates appeared where input A was sufficiently large to trigger saturated polarization, whereas input B remained low, leaving the polarization unaffected. Xfer B gates occurred when input B was sufficiently large to induce saturated polarization, overriding the influence of input A. These findings confirm that the logic gates functioned as anticipated, correlating with the input amplitudes and the resulting polarization responses. A more detailed analysis of the current variations shown in the current maps in Figure 4d(i,iii), as well as the optimal conditions for inputs A and B, is available in Note S1. Compared with conventional CMOS technology, which requires at least four transistors for AND or OR circuits, the proposed vdW FeFET-based S-LiM unit significantly reduces circuit complexity, minimizes static power dissipation, and uses fewer transistors, leading to more efficient designs. Furthermore, the comparison of memory-based sequential Boolean Logic Units is shown in Table S1. FeFET-based devices offer significant advantages in circuit design through their reconfigurability, enabling dynamic adaptability, efficient resource use, and flexible functionality. They allow devices to switch between logic functions, such as AND and OR, based on processing needs, making them suitable for applications in edge computing and IoT, which handle varied tasks like filtering and pattern recognition. This adaptability reduces the need for multiple dedicated circuits, allowing a single hardware component to perform diverse functions. FeFETs also increase space efficiency by consolidating multiple logic functions into one component through polarization states, leading to compact designs ideal for wearable and implantable devices. Moreover, their reconfigurability aligns well with traditional programmable logic arrays and field-programmable gate arrays and even has the potential to replace them, as FeFETs can enable multifunctional logic blocks that are adaptable postfabrication, supporting task-specific customization in programmable circuits.

2.4. Application of Low-Power Edge Device/Computing. Based on the above discussion, the reconfigurable S-LiM achieved in the energy- and area-efficient vdW FeFET demonstrates significant potential for low-power edge computing applications. As shown in Figure 5a, in many IoT systems, vast amounts of data generated by various sensors are

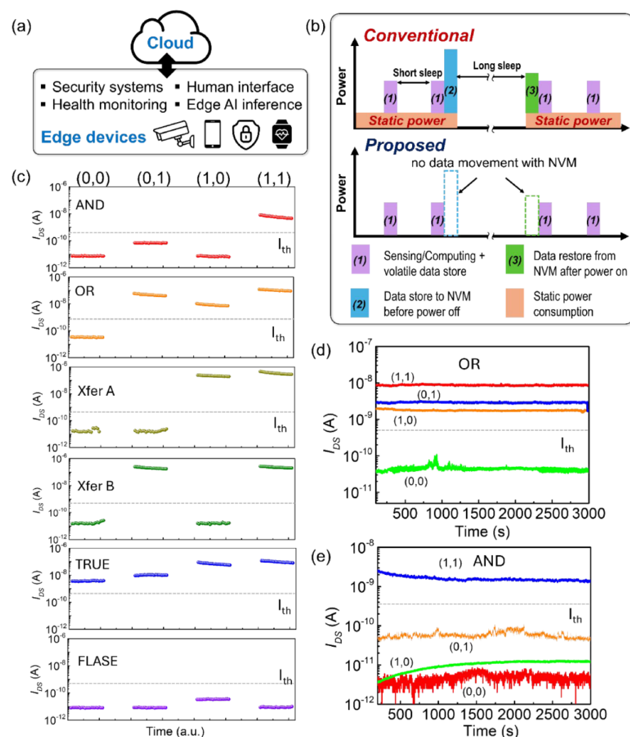

Figure 5. (a) Conceptual drawing of IoT and edge computing. (b) Schematic comparison for the conventional sequential logic and proposed reconfigurable S-LiM unit working process. (c) I_{DS} versus time for six Boolean logic functions (TRUE, FALSE, OR, AND, Xfer A, and Xfer B) performed using a single vdW FeFET with sequential input pulses. (d, e) Long-term retention and fast recovery of logic operations (d) OR and (e) AND.

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processed and optimized by edge computing devices before being transferred to central or cloud computing systems.[36] These edge computing devices typically have limited power and energy budgets because they often rely on batteries as energy sources. They are often deployed in remote locations without stable wired power sources, which makes replacing batteries costly. Therefore, they must be highly energy-efficient to operate solely on battery power or rely on self-powering methods, such as environmental energy harvesting.[36] These devices maintain low activity to minimize the operational energy cost by duty-cycling. This involves intermittently powering up to take measurements, processing and storing measured data, and powering down until the next triggering event or specific conditions are met. Figure 5b shows how the system-level operation of an edge computing device can potentially be improved by using the proposed vdW FeFET-based S-LiM unit. An edge computing device is periodically activated for data collection (process (1)); with each activation, measurements are taken with sensors, and the processed data are temporarily stored in volatile memory. The system can be powered on with minimal operational power if the next activation is expected within a short time window (short sleep). However, static power is consumed to maintain the data in the volatile memory. After the next activation, if the subsequent activations are expected to be far apart, the entire system must be powered off to save energy (long sleep). Before powering off, data must be transferred to NVM (process (2)) to prevent loss, which may incur large energy consumption owing to the high write energy of a typical NVM. After power restoration, data must be restored from the NVM (process (3)) and transferred back to the logic circuit for recovery and start-up, incurring additional time and energy costs.

With the proposed vdW FeFET-based S-LiM unit, these duty-cycling processes can be significantly simplified. Owing to the nonvolatile nature of data storage using ferroelectric polarization, the data processed with the S-LiM unit are effectively stored with NVM immediately after processing. Therefore, power can be turned off without transferring data to an external NVM, ensuring data retention while eliminating both static energy consumption and overhead for data storage/restoration. The in situ memory property allows for rapid recovery and startup without additional data readout processes once the edge computing device is reactivated. Figure 5c illustrates I_{DS} versus time for six Boolean logic functions (Logic High, Logic Low, OR, AND, Xfer A, and Xfer B) performed by using a single vdW FeFET with sequential input pulses. The observed I_{DS}-level differences of >10^3 for most logic operations highlight the robust performance of 1T sequential logic gates. Figure 5d,e shows the long-term I_{DS} measurements obtained immediately after the second input V_{GSB} was turned off. The logic AND and OR operations, which are widely used in practical logic circuits, were also tested. These results robustly demonstrate the exceptional long-term memory capability of the device, validating its suitability for environments with intermittent power supplies. Remarkably, even after 3000 s of power-off, the conductance states of the device exhibited virtually no relaxation, underscoring its outstanding stability. This stability highlights the reliability of the device for sequential logic operations and its effectiveness in edge computing devices. In both cases, the device maintained stable conductance states postoperatively, underscoring its ability to recover quickly, even after extended power-off periods. Future research on FeFET-based (or even with other types of device-based) reconfigurable logic could focus on expanding available logic functions and enhancing compatibility with CMOS technology. First, implementing a wider range of logic functions, such as NAND, NOR, XOR, and INV, would make FeFET-based gates even more versatile. By broadening the set of available functions, complex logic operations can be simplified, allowing for more compact circuit designs tailored to specific applications. Additionally, exploring the implementation of "voltage mode" logic functions in FeFET devices could increase their compatibility with CMOS technology, which primarily operates in voltage mode. Currently, FeFET devices perform logic in "current mode", where different current levels represent logic states. Shifting to the voltage mode would make FeFET circuits more integrative with the existing CMOS digital designs, opening up new avenues for seamless integration in modern electronic systems.

3. CONCLUSION

This study has demonstrated an approach that integrates compact, nonvolatile, and reconfigurable sequential logic gates within a single vdW FeFET. This innovative design achieves reconfigurable S-LiM in an energy- and area-efficient manner. The device supports six distinct logic operations via voltage-controlled ferroelectric polarization. Its capability to store data internally without requiring external transfers and to rapidly recover and restart makes it ideal for low-power edge computing applications. This device represents a significant advancement in computing technologies and architectures, promising both efficiency and versatility.

4. EXPERIMENTAL SECTION

4.1. Device Fabrication. A bottom gate terminal was deposited via electron-beam evaporation after patterning by using electron-beam lithography. Bulk MoS_2 was purchased from 2D Semiconductors and bulk CIPS was purchased from HQ Graphene. Thin MoS_2 and CIPS flakes were obtained by mechanical exfoliation and then transferred onto the bottom gate by using the dry transfer method. The source and drain electrodes were patterned using electron-beam lithography, followed by the deposition of Ti/Au (10 nm/80 nm) using e-beam evaporation.

4.2. Device and Material Characterization. An optical microscope (Olympus, BX51M) was used to confirm the size and shape of the flakes and devices. The thickness of the thin flakes was measured using atomic force microscopy (AFM; Park-NX10, M/s Park Systems Corp.) in noncontact mode. Standard PFM measurements used the same AFM system in contact mode. A conductive tip with Cr/Pt coating was selected (Multi75E-G, BudgetSensors; tip radius = 25 nm, spring constant $k \approx 3$ N m^{-1}, resonance frequency $f \approx 75$ kHz). The frequency and amplitude of the alternating voltage V_{ac} for the PFM image characterization studies were 17 kHz and 4 V, respectively. Single-point piezoresponse hysteresis loops were collected using a combination of a changing DC bias and a 4 V AC bias. All of the electrical characterizations were performed using a Keithley 4200 semiconductor characterization system (M/s, Tektronix Inc.) at room temperature. During electrical characterization, the device was placed in the atmosphere. Raman spectroscopy was performed by using a Raman spectrometer (WITEC Alpha 300M) with a 532 nm laser. Cross-sectional transmission

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electron microscopy (TEM; JEOL, JEM ARM 200F) measurements were performed for the structural analysis.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.4c14062.

Comparison of memory-based sequential Boolean logic units; CMOS-based sequential logic circuit and proposed vdW FeFET-based S-LiM unit; AFM image and height profiles of the FeFET; PFM measurement of CIPS flake; polarization-electric field measurement of a typical CIPS capacitor; hysteresis characteristics of the vdW FeFET; energy band diagrams for the vdW FeFET; PFM scanning of the channel area of the vdW FeFET; comparison with other reported vdW FeFET NVM (PDF)

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Notes

The authors declare no competing financial interest.

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